1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Mullet

M1 MLB
09/26/2005

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

Page (.csa)	Contents	Sync	Date
1 1	Table of Contents	N/A	N/A
2 2	System Block Diagram	N/A	N/A
3 3	Power Block Diagram	N/A	N/A
4 4	BOM Configuration	N/A	N/A
5 5	Functional / ICT Test	N/A	N/A
6 6	Signal Aliases	N/A	N/A
7 7	CPU 1 OF 2-FSB	M42	09/08/2005
8 8	CPU 2 OF 2-PWR/GND	M42	09/08/2005
9 9	CPU Decoupling & VID	(MASTER)	(MASTER)
10 10	CPU MISC1-TEMP SENSOR	M42	09/08/2005
11 11	CPU ITP700FLEX DEBUG	M42	09/08/2005
12 12	NB CPU Interface	(MASTER)	(MASTER)
13 13	NB PEG / Video Interfaces	(MASTER)	(MASTER)
14 14	NB Misc Interfaces	(MASTER)	(MASTER)
15 15	NB DDR2 Interfaces	(MASTER)	(MASTER)
16 16	NB Power 1	(MASTER)	(MASTER)
17 17	NB Power 2	(MASTER)	(MASTER)
18 18	NB Grounds	(MASTER)	(MASTER)
19 19	NB (GM) Decoupling	(MASTER)	(MASTER)
20 20	NB Config Straps	(MASTER)	(MASTER)
21 21		M38	09/08/2005
22 22		M38	09/08/2005
23 23		M38	09/08/2005
24 24		M38	09/08/2005
25 25		M42	09/08/2005
26 26	SB Misc	(MASTER)	(MASTER)
27 27	M1 SMBus Connections	(MASTER)	(MASTER)
28 28	DDR2 SO-DIMM Connector A	(MASTER)	(MASTER)
29 29	DDR2 SO-DIMM Connector B	(MASTER)	(MASTER)
30 30	Memory Active Termination	(MASTER)	(MASTER)
31 31	Memory Vtt Supply	(MASTER)	(MASTER)
32 32	DDR2 VRef	(MASTER)	(MASTER)
33 33	CLOCKS	M42	09/08/2005
34 34	Clock Termination	(MASTER)	(MASTER)
35 37	Mobile Clocking	(MASTER)	(MASTER)
36 38	PATA Connector	(MASTER)	(MASTER)
37 41	ETHERNET CONTROLLER	M42	09/08/2005
38 42	Ethernet Connector	(MASTER)	(MASTER)
39 44	FIREWIRE CONTROLLER	M42	08/29/2005
40 45	FireWire Port Power	(MASTER)	(MASTER)
41 46	FireWire Ports	(MASTER)	(MASTER)
42 49	Internal USB Connections	(MASTER)	(MASTER)
43 52	External USB Connector	(MASTER)	(MASTER)
44 55	Left I/O Board Connector	(MASTER)	(MASTER)
45 57	PCI-E Connections	(MASTER)	(MASTER)
46 58		M38	09/08/2005
47 59	SMC Support	(MASTER)	(MASTER)
48 60	LPC+ Debug Connector	M42	07/20/2005
49 61	Thermal Sensors	(MASTER)	(MASTER)
50 62	Current & Voltage Sensing	(MASTER)	(MASTER)
51 63	SPI BOOTROM	(M42)	07/26/2005
52 64	ALS Support	(MASTER)	(MASTER)
53 65	Fan Connectors	(MASTER)	(MASTER)
54 66	SMS	(M42)	07/26/2005
55 67		M38	09/08/2005
56 75	IMVP6 CPU VCore Regulator	(MASTER)	(MASTER)
57 76	5V / 1.5V Power Supply	(MASTER)	(MASTER)
58 77	2.5V & 1.2V Regulators	(MASTER)	(MASTER)
59 78	1.8V Supply	(MASTER)	(MASTER)
60 79	3.3V / 1.05V Power Supplies	(MASTER)	(MASTER)
61 80	3.3V G3Hot Supply	(MASTER)	(MASTER)
62 81	Power Aliases	(MASTER)	(MASTER)
63 82	PBus-In & Battery Connectors	(MASTER)	(MASTER)
64 83	S3/S0 FETs & Power Control	(MASTER)	(MASTER)
65 84	ATI M56 PCI-E	(MASTER)	(MASTER)
66 85	GPU (M56) Core Supplies	(MASTER)	(MASTER)
67 86	ATI M56 Core Power	(MASTER)	(MASTER)
68 87	ATI M56 Frame Buffer I/F	(MASTER)	(MASTER)
69 88	GPU Straps	(MASTER)	(MASTER)
70 89	GDDR3 Frame Buffer A	(MASTER)	(MASTER)
71 90	GDDR3 Frame Buffer B	(MASTER)	(MASTER)
72 91	ATI M56 GPIO/DVO/Misc	(MASTER)	(MASTER)
73 93	ATI M56 Video Interfaces	(MASTER)	(MASTER)
74 94	Internal Display Connectors	(MASTER)	(MASTER)
75 97	External Display Connector	(MASTER)	(MASTER)
76 99	Physical Security	(MASTER)	(MASTER)
77 100	Revision History	N/A	N/A
78 101	Napa Platform Constraints	(MASTER)	(MASTER)
79 102	More System Constraints	(MASTER)	(MASTER)
80 103	M1 Spacing & Physical Constraints	(MASTER)	(MASTER)
81 104	M1 Net Properties	(MASTER)	(MASTER)

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM,MULLET,M1	SCH		
820-1881	1	PCBF,MULLET,M1	PCB		
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TSQ]	CRITICAL	VRAM_128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TYY]	CRITICAL	VRAM_256

DRAWING
TITLE=MULLET
ABBREV=DRAWING
LAST_MODIFIED=Mon Sep 26 13:38:08 2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE
SCHEM,MULLET,M1

DRAWING NUMBER 051-6941 REV. 07001

SHT 1 OF 81

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8 7 6 5 4 3 2 1

D C B A

System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

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J5500
LIO Flex Connector
PPDCIN_G3H
18.5V - 9V
U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V
J8200
LIO Power Connector
PPBUS_G3H_B
12.6V - 9V
PPBUS_G3H_A
12.6V - 9V
SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
U7600
ENABLES
5V/1.5V S5/S0 (LTC3728)
PGOOD
PP5V_S5
5.0V
PP1V5_S0
1.5V
NC
Q8300
PP5V_S3
5.0V
PM_SLP_S4_LS5V
Q8305
PP5V_S0
5.0V
PM_SLP_S3_LS5V
IMVP_VR_ON
IMVP_PWRGD_IN
U7500
ENABLES
CPU VCore S0 (ISL6262) "IMVP6"
PGOOD
PPVCORE_S0_CPU
?V
VR_PWRGOOD_DELAY
J5500
Inverter Connector
PM_SLP_S4_L
U7800
ENABLE
1.8V S3 (ISL6269)
PGOOD
PP1V8_S3
1.8V
NC
SMC_PM_G2_ENABLE
U7900
ENABLE
3.3V S5 (ISL6269)
PGOOD
PP3V3_S5
3.3V
RSMRST_PWRGD
PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269)
PGOOD
PP1V05_S0
1.05V
IMVP_PWRGD_IN/ALL_SYS_PWRGD
PM_SLP_S3_L
U8500
ENABLE
GPU VCore S0 (ISL6269)
PGOOD
PPVCORE_S0_GPU
1.2V - 1.0V
NC
Q8310
PP3V3_S3
3.3V
PM_SLP_S4_LS5V
U7700
ENABLE
2.5V S3 (LTC3411)
PGOOD
PP2V5_S3
2.5V
NC
Q8320
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L
U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
PP1V2_S3
1.2V
NC
Q8330
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L
Q8315
PP3V3_S0
3.3V
PM_SLP_S3_LS5V
PM_SLP_S3_L
U3100
ENABLE
0.9V (Vtt) S0 (BD3533FVM)
PP0V9_S0
0.9V
Q8325
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L
Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

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BOM NUMBER	BOM NAME	BOM OPTIONS
630-7207	PCBA,MULLET_128,M1	075-0137,075-0139,075-0140
630-7254	PCBA,MULLET_256,M1	075-0138,075-0139,075-0140
075-0137	128,MULLET,M1	VRAM_128
075-0138	256,MULLET,M1	VRAM_256,GPU_MEM_256M
075-0139	PROJ_PTS,MULLET,M1	COMMON,M1_COMMON1,M1_COMMON2,M1_DEBUG
075-0140	LEMENU_PTS,MULLET,M1	LEMENU_STAGE2,LEMENU_STAGE3

BOM GROUP	BOM OPTIONS
M1_COMMON1	GPU_BB_CTL,GPUTHM_A_GPU,HSTHMSNS_HAS,INVERTER_BUF,KBDLED_HAS,LEMENU_STAGE1
M1_COMMON2	MEMVREF_S3,MEMVTT_EN_PU,PLTRST_GATE_STUFF,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M1_DEBUG	DEVELOPMENT,ITP,LPCPLUS

Phantom BOM #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
075-0137	1	128,MULLET,M1	BOM1		075-0137
075-0138	1	256,MULLET,M1	BOM2		075-0138
075-0139	1	PROJ PTS,MULLET,M1	BOM3		075-0139
075-0140	1	LeMENU PTS,MULLET,M1	BOM4		075-0140

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256

"LeMenu Stage #1" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
338S0266	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	LEMENU_STAGE1	
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	CRITICAL	LEMENU_STAGE1	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	LEMENU_STAGE1	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	LEMENU_STAGE1	
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	LEMENU_STAGE1	
341S1812	1	IC,EFI,BOOTROM DEVELOPMENT,M1	U6301	CRITICAL	LEMENU_STAGE1	341S1813 is production BootROM
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	LEMENU_STAGE1	
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	LEMENU_STAGE1	

"LeMenu Stage #2" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	LEMENU_STAGE2

"LeMenu Stage #3" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3208	1	IC,YONAH CPU,479 BGA	U0700	CRITICAL	LEMENU_STAGE3
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	LEMENU_STAGE3
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	LEMENU_STAGE3

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

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Functional Test Points

Power Supply NO_TESTs

NO_TEST

TRUE	IMVP6_RBIAS	56
TRUE	IMVP6_COMP	56
TRUE	P5VS5_RUNSS	57 64
TRUE	P1V5S0_RUNSS	57 64
TRUE	P2V5S3_MODE	58
TRUE	P2V5S3_SHDNRT	58 64
TRUE	P1V2S3_RT	58
TRUE	P1V2S3_RUNSS	58 64
TRUE	P1V8S3_COMP	59
TRUE	P1V8S3_FSET	59
TRUE	P3V3S5_COMP	60
TRUE	P3V3S5_FSET	60
TRUE	P1V05S0_COMP	60
TRUE	P1V05S0_FSET	60
TRUE	P3V42G3H_FB	61
TRUE	GPUVCORE_COMP	66
TRUE	GPUVCORE_FSET	66
TRUE	GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	7 12 81
TRUE	FSB_ADS_L	7 12 81
TRUE	FSB_ADSTB_L<1..0>	7 12 81
TRUE	FSB_BNR_L	7 12 81
TRUE	FSB_BREQ0_L	7 12 81
TRUE	FSB_D_L<63..0>	7 12 81
TRUE	FSB_DBSY_L	7 12 81
TRUE	FSB_DINV_L<3..0>	7 12 81
TRUE	FSB_DRDY_L	7 12 81
TRUE	FSB_DSTBN_L<3..0>	7 12 81
TRUE	FSB_DSTBP_L<3..0>	7 12 81
TRUE	FSB_HIT_L	7 12 81
TRUE	FSB_HITM_L	7 12 81
TRUE	FSB_LOCK_L	7 12 81
TRUE	FSB_REQ_L<4..0>	7 12 81

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST

	=PP5V_S0_FAN_LT	53 62
	FAN_LT_PWM	53
	FAN_LT_TACH	53
	FAN_RT_PWM	53
	FAN_RT_TACH	53

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	48 62
TRUE	=PP5V_S0_LPCPLUS	48 62
TRUE	LPC_AD<0>	21 46 48 55
TRUE	LPC_AD<1>	21 46 48 55
TRUE	LPC_FRAME_L	21 46 48 55
TRUE	PM_CLKRUN_L	23 39 46 48 55
TRUE	BOOT_LPC_SPI_L	22 46 48 76
TRUE	SMC_TMS	46 47 48
TRUE	DEBUG_RST_L	26 48
TRUE	SMC_TRST_L	46 48
TRUE	SMC_TDO	46 47 48
TRUE	SMC_MD1	46 48
TRUE	SMC_TX_L	46 47 48
TRUE	FWH_INIT_L	21 47 48
TRUE	PCI_CLK_PORT80_LPC	34 48
TRUE	LPC_AD<2>	21 46 48 55
TRUE	LPC_AD<3>	21 46 48 55
TRUE	INT_SERIRQ	23 46 48 55
TRUE	PM_SUS_STAT_L	23 46 48 55
TRUE	SMC_TDI	46 47 48
TRUE	SMC_TCK	46 47 48
TRUE	SMC_RST_L	46 47 48
TRUE	SMC_NMI	46 48
TRUE	SMC_RX_L	46 47 48
TRUE	SV_SET_UP	23 48

Other Func Test Points

FUNC_TEST

TRUE	=PP1V05_S0_REG	50 60 62

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	46 47 63
TRUE	=SMBUS_BATT_SCL	27 63
TRUE	=SMBUS_BATT_SDA	27 63
TRUE	GND_BATT	63

Left I/O Data Connector

FUNC_TEST

TRUE	=PP1V5_S0_LIO	44 62
TRUE	=PPDCIN_G3H_LIO	44 62
TRUE	=PP5V_S5_LIO	44 62
TRUE	=PP3V42_G3H_LIO	44 62
TRUE	PP5V_S0_AUDIO_PWR	44
TRUE	PP5V_S0_AUDIO	44
TRUE	GND_AUDIO_PWR	44
TRUE	GND_AUDIO	44
TRUE	ACZ_SDATAIN<0>	21 44 81
TRUE	ACZ_SDATAOUT	21 44 81
TRUE	ACZ_BITCLK	21 44 81
TRUE	ACZ_RST_L	21 44 81
TRUE	EXCARD_OC_L	6 44 47
TRUE	LTUSB_OC_L	6 44
TRUE	LIO_BATT_ISENSE	44 50
TRUE	SMC_SYS_ISET	44 46
TRUE	SMC_BATT_ISET	44 46
TRUE	SMC_BATT_CHG_EN	44 46 47
TRUE	SMC_BC_ACOK	44 46 47
TRUE	SMC_ADAPTER_EN	40 44 46 47
TRUE	LIO_P3V3S0_EN_L	44 64
TRUE	LIO_DCIN_ISENSE	44 50
TRUE	LIO_P3V3S3_EN	44 64
TRUE	SMC_BATT_TRICKLE_EN_L	44 46 47
TRUE	SYS_ONEWIRE	44 46 47
TRUE	MINI_CLKREQ_L	34 44
TRUE	SMC_EXCARD_CP	44 46 47
TRUE	EXCARD_CLKREQ_L	34 44
TRUE	SMC_EXCARD_PWR_EN	44 46
TRUE	LIO_PLT_RESET_L	26 44
TRUE	ACZ_SYNC	21 44 81
TRUE	=USB2_LT_N	6 44
TRUE	=USB2_LT_P	6 44
TRUE	=USB2_EXCARD_N	6 44
TRUE	=USB2_EXCARD_P	6 44
TRUE	=PCIE_EXCARD_R2D_N	44 45
TRUE	=PCIE_EXCARD_R2D_P	44 45
TRUE	=PCIE_EXCARD_D2R_N	44 45
TRUE	=PCIE_EXCARD_D2R_P	44 45
TRUE	PCIE_CLK100M_EXCARD_P	34 44
TRUE	PCIE_CLK100M_EXCARD_N	34 44
TRUE	=USB2_MINI_N	6 44
TRUE	=USB2_MINI_P	6 44
TRUE	=PCIE_MINI_R2D_N	44 45
TRUE	=PCIE_MINI_R2D_P	44 45
TRUE	=PCIE_MINI_D2R_N	44 45
TRUE	=PCIE_MINI_D2R_P	44 45
TRUE	PCIE_CLK100M_MINI_P	34 44
TRUE	PCIE_CLK100M_MINI_N	34 44
TRUE	=SMBUS_LIO_SMC_SCL	27 44
TRUE	=SMBUS_LIO_SMC_SDA	27 44
TRUE	=SMBUS_LIO_SB_SCL	27 44
TRUE	=SMBUS_LIO_SB_SDA	27 44
TRUE	PCIE_WAKE_L	23 37 44

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	62 63
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

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NONE	5	81

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NC_CPU_A32_L = TP_CPU_A32_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_A33_L = TP_CPU_A33_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_A34_L = TP_CPU_A34_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_A35_L = TP_CPU_A35_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_A36_L = TP_CPU_A36_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_A37_L = TP_CPU_A37_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_A38_L = TP_CPU_A38_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_A39_L = TP_CPU_A39_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_APM0_L = TP_CPU_APM0_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_APM1_L = TP_CPU_APM1_L (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_EXTBREF = TP_CPU_EXTBREF (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_HFPLL = TP_CPU_HFPLL (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_SPARE0 = TP_CPU_SPARE0 (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_SPARE1 = TP_CPU_SPARE1 (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_SPARE2 = TP_CPU_SPARE2 (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_CPU_SPARE4 = TP_CPU_SPARE4 (7)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_MEM_A_A<15..14> = MEM_A_A<15..14> (28)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_MEM_B_A<15..14> = MEM_B_A<15..14> (29)
MAKE_BASE=TRUE
NO_TEST=TRUE

TP_NB_CFG<4..3> = NB_CFG<4..3> (14)
MAKE_BASE=TRUE

TP_NB_CFG<6> = NB_CFG<6> (14)
MAKE_BASE=TRUE

TP_NB_CFG<8> = NB_CFG<8> (14)
MAKE_BASE=TRUE

TP_NB_CFG<11..10> = NB_CFG<11..10> (14)
MAKE_BASE=TRUE

TP_NB_CFG<15..14> = NB_CFG<15..14> (14)
MAKE_BASE=TRUE

TP_NB_CFG<17> = NB_CFG<17> (14)
MAKE_BASE=TRUE

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> = NB_CFG<13..12> (14)
MAKE_BASE=TRUE

TP_SB_SUS_CLK = SUS_CLK_SB (23)
MAKE_BASE=TRUE

NC_ENET_CTRL12 = ENET_CTRL12 (37)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_ENET_CTRL25 = ENET_CTRL25 (37)
MAKE_BASE=TRUE
NO_TEST=TRUE

NC_FWPWR_PWRON = =FWPWR_PWRON (40)
MAKE_BASE=TRUE
NO_TEST=TRUE

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P = USB2_RT_P (43) = USB_A_P (22)
MAKE_BASE=TRUE

=USB2_RT_N = USB2_RT_N (43) = USB_A_N (22)
MAKE_BASE=TRUE

=RTUSB_OC_L = RTUSB_OC_L (43) = USB_A_OC_L (22)
MAKE_BASE=TRUE

USB Port "B" = PCI-E Mini Card

=USB2_MINI_P = USB2_MINI_P (44,5) = USB_B_P (22)
MAKE_BASE=TRUE

=USB2_MINI_N = USB2_MINI_N (44,5) = USB_B_N (22)
MAKE_BASE=TRUE

UNUSED_USB_B_OC_L = USB_B_OC_L (22)
MAKE_BASE=TRUE

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P = USB2_LT_P (44,5) = USB_C_P (22)
MAKE_BASE=TRUE

=USB2_LT_N = USB2_LT_N (44,5) = USB_C_N (22)
MAKE_BASE=TRUE

LTUSB_OC_L = USB_C_OC_L (44,5) (22)
MAKE_BASE=TRUE

USB Port "D" = Camera

=USB2_CAMERA_P = USB2_CAMERA_P (42) = USB_D_P (22)
MAKE_BASE=TRUE

=USB2_CAMERA_N = USB2_CAMERA_N (42) = USB_D_N (22)
MAKE_BASE=TRUE

UNUSED_USB_D_OC_L = USB_D_OC_L (22)
MAKE_BASE=TRUE

USB Port "E" = ExpressCard

=USB2_EXCARD_P = USB2_EXCARD_P (44,5) = USB_E_P (22)
MAKE_BASE=TRUE

=USB2_EXCARD_N = USB2_EXCARD_N (44,5) = USB_E_N (22)
MAKE_BASE=TRUE

EXCARD_OC_L (47,44,5) = USB_E_OC_L (22)
MAKE_BASE=TRUE

USB Port "F" = IR Receiver

=USB_IR_P = TP_USB_IRP = USB_F_P (22)
MAKE_BASE=TRUE

=USB_IR_N = TP_USB_IRN = USB_F_N (22)
MAKE_BASE=TRUE

USB Port "G" = Bluetooth (M13P)

=USB_BT_P = USB_BT_P = USB_G_P (22)
MAKE_BASE=TRUE

=USB_BT_N = USB_BT_N = USB_G_N (22)
MAKE_BASE=TRUE

USB Port "H" = Trackpad (Geyser)

=USB_TRACKPAD_P = USB_TRACKPAD_P = USB_H_P (22)
MAKE_BASE=TRUE

=USB_TRACKPAD_N = USB_TRACKPAD_N = USB_H_N (22)
MAKE_BASE=TRUE

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
1

GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_DVI_TOP = =GND_CHASSIS_DVI2 (75)
GND_CHASSIS_DVI_TOP = =GND_CHASSIS_DVI4 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
1

GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_DVI_BOT = =GND_CHASSIS_DVI1 (75)
GND_CHASSIS_DVI_BOT = =GND_CHASSIS_DVI3 (75)
GND_CHASSIS_DVI_BOT = =GND_CHASSIS_ENET (38)
GND_CHASSIS_DVI_BOT = =GND_CHASSIS_FW_EMI (41)
GND_CHASSIS_DVI_BOT = =GND_CHASSIS_FW_PORT1 (41)
GND_CHASSIS_DVI_BOT = =GND_CHASSIS_RTUSB (43)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
1

GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_LVDS = =GND_CHASSIS_LCD1 (74)
GND_CHASSIS_LVDS = =GND_CHASSIS_LCD2 (74)
GND_CHASSIS_LVDS = =GND_CHASSIS_LCD3 (74)
GND_CHASSIS_LVDS = =GND_CHASSIS_LCD4 (74)

SH0600
OG-503040
SHLD-SM-LF
1
2
3

GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_INVERTER = =GND_CHASSIS_INVERTER (74)

Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	6	81

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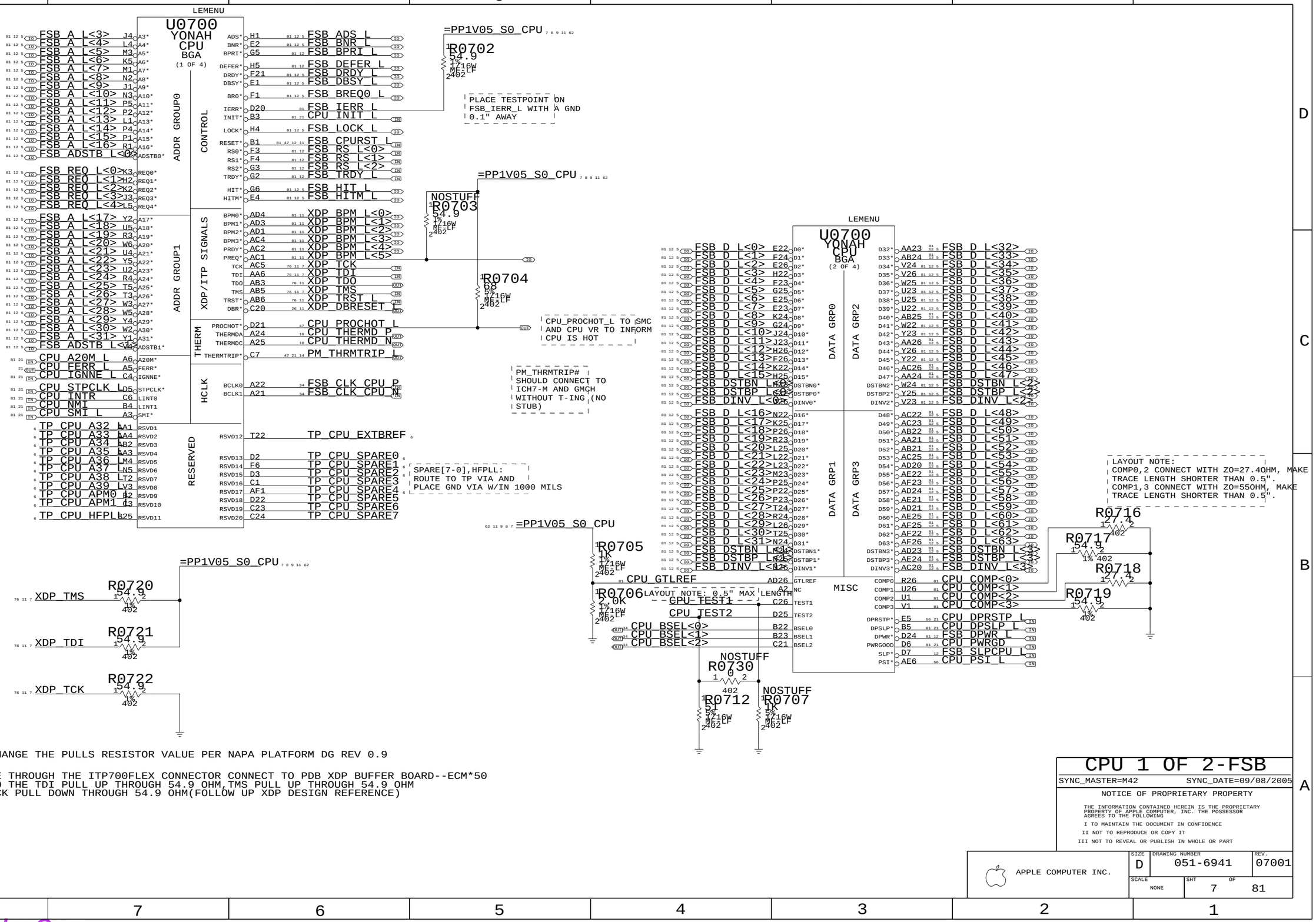

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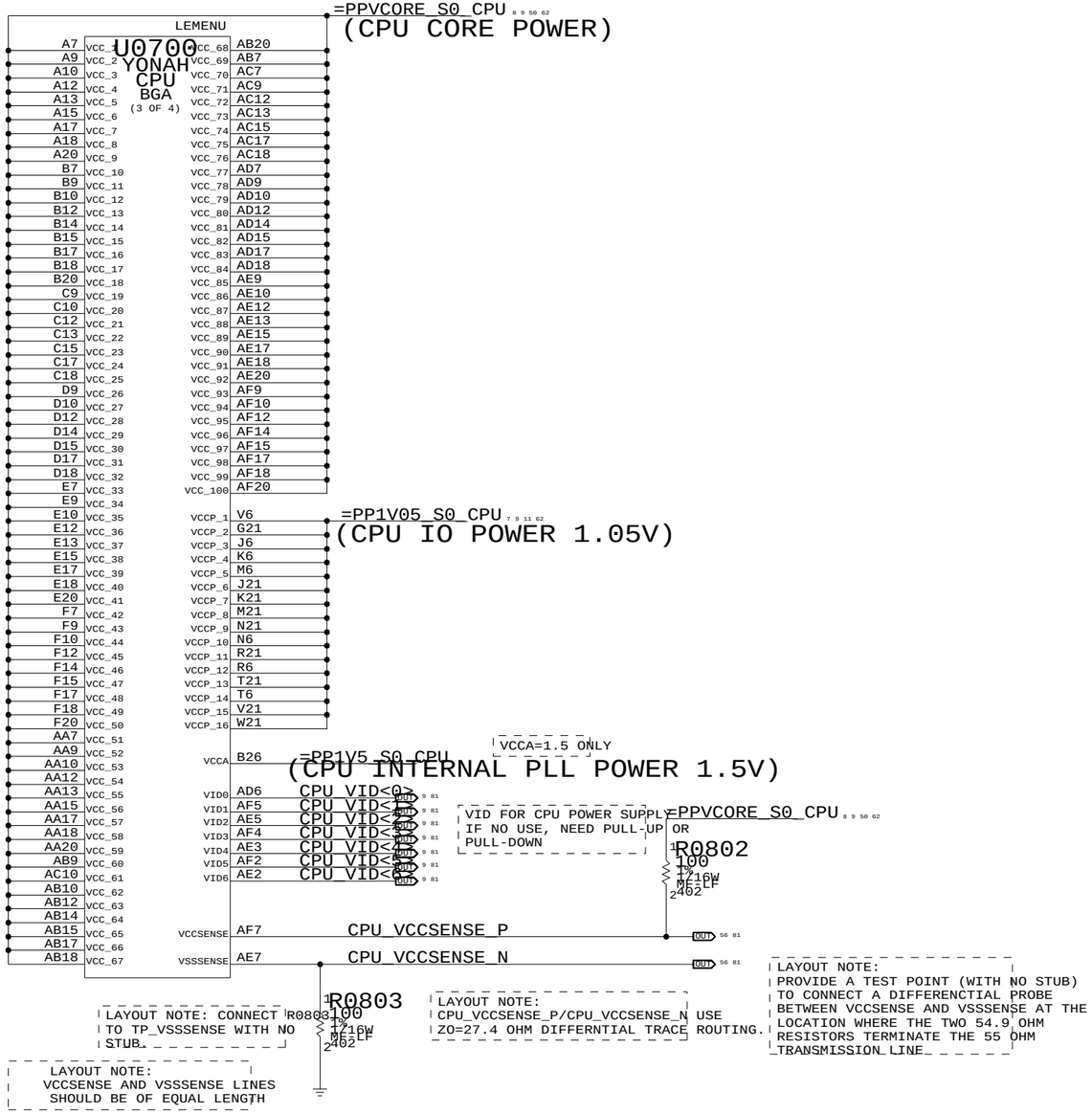

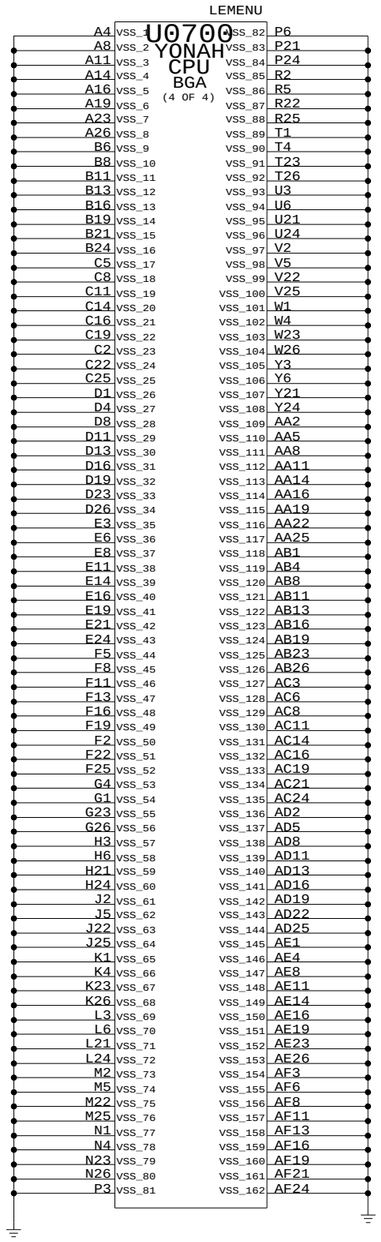

CPU 2 OF 2-PWR/GND

SYNC_MASTER=M42 SYNC_DATE=09/08/2005

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NONE	8	81

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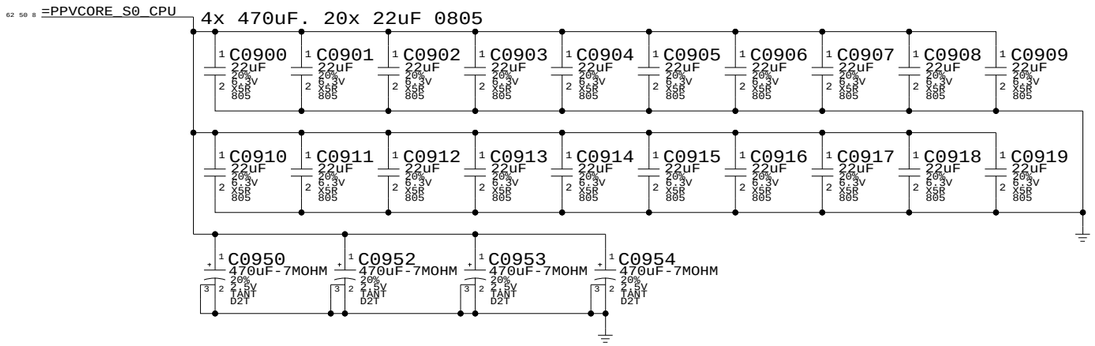
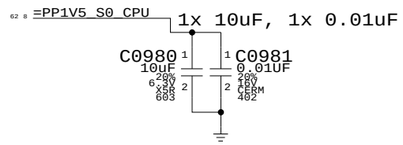
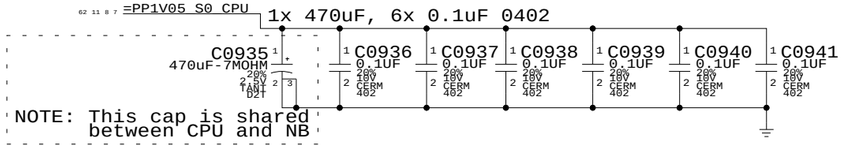
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

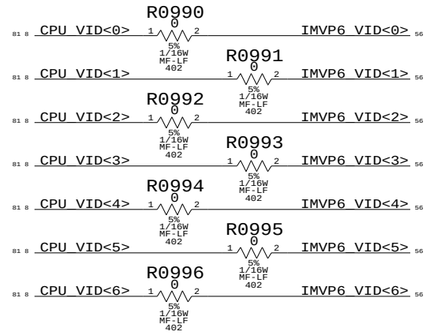


VCCP (CPU I/O) Decoupling


62 11 8 7 =PP1V05_S0_CPU
1x 470uF, 6x 0.1uF 0402
C0935 470uF-7MOHM 20% 2.5V TANT D2T
C0936 C0937 C0938 C0939 C0940 C0941
0.1UF 20% 16V CERM 402
NOTE: This cap is shared between CPU and NB

CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	9	81

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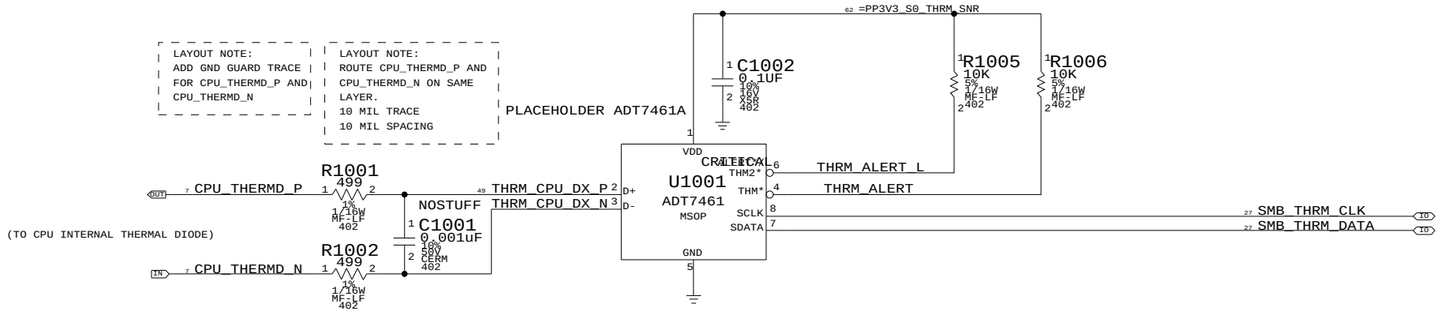
CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

SYNC_MASTER=M42 SYNC_DATE=09/08/2005

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NONE	10	81

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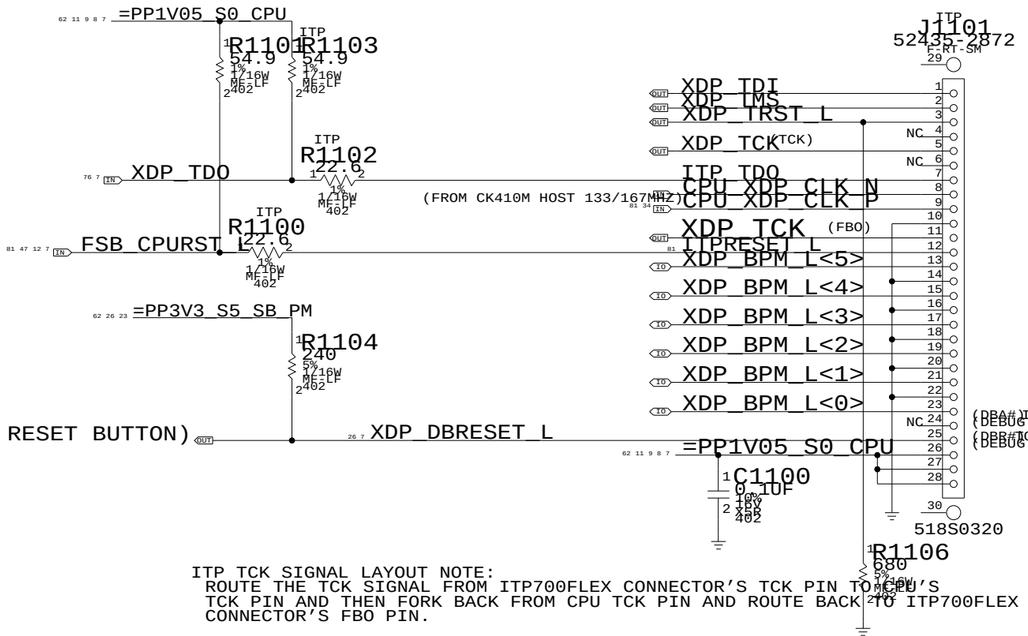
CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M52 SYNC_DATE=09/08/2005

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	SCALE: NONE	SHT 11 OF 81	

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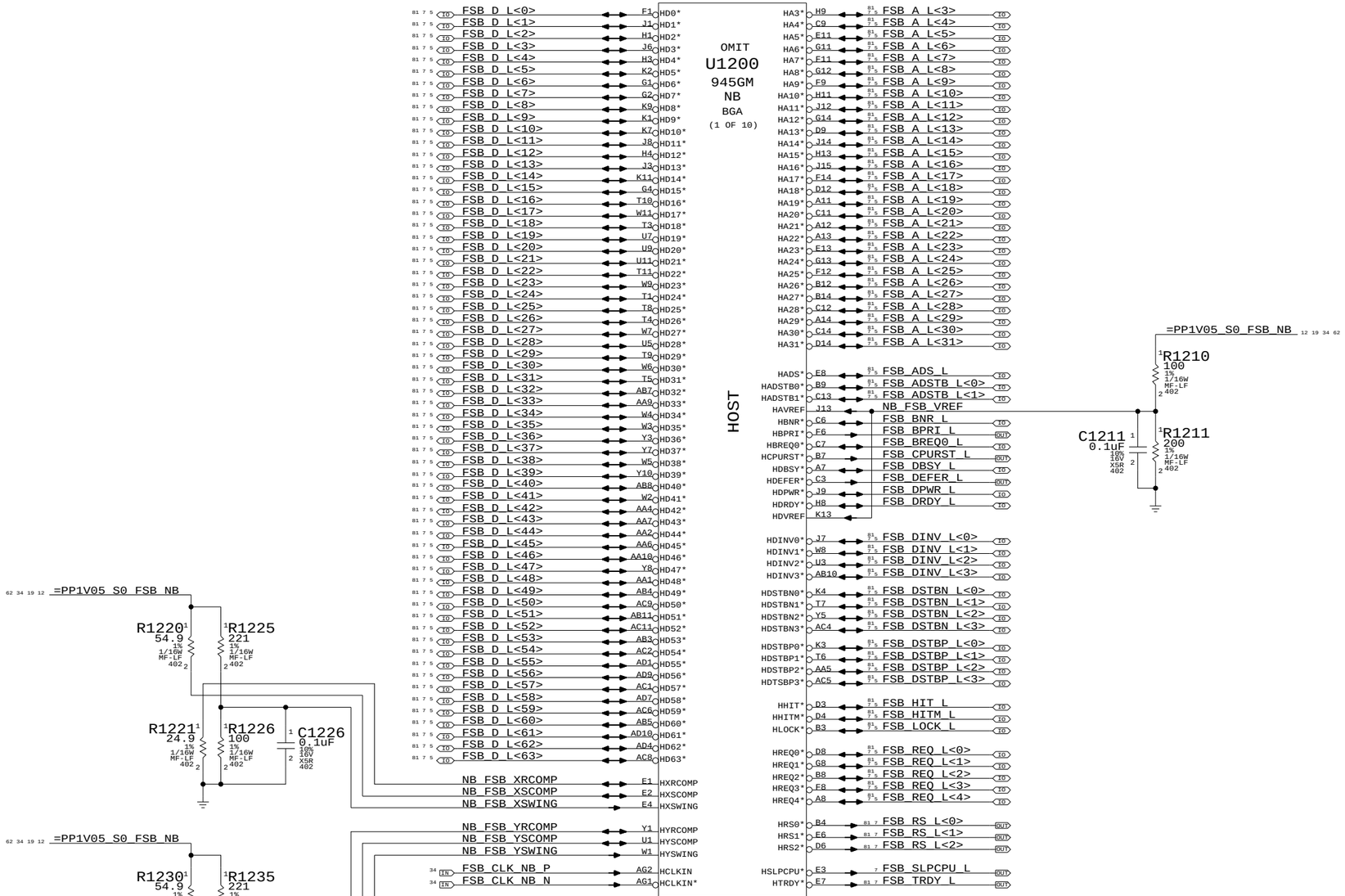

NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	12	81

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

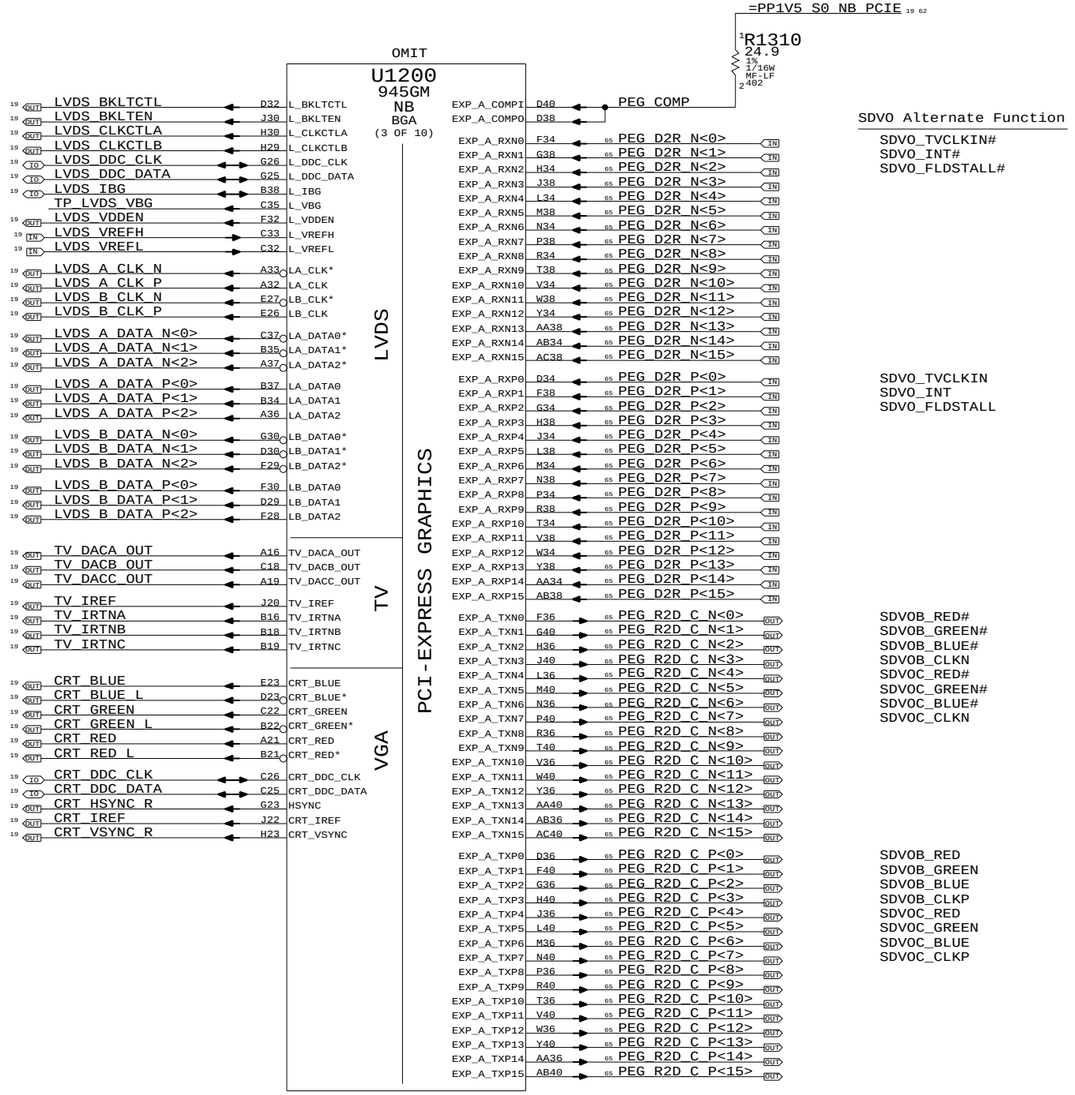
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail. Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	13	81

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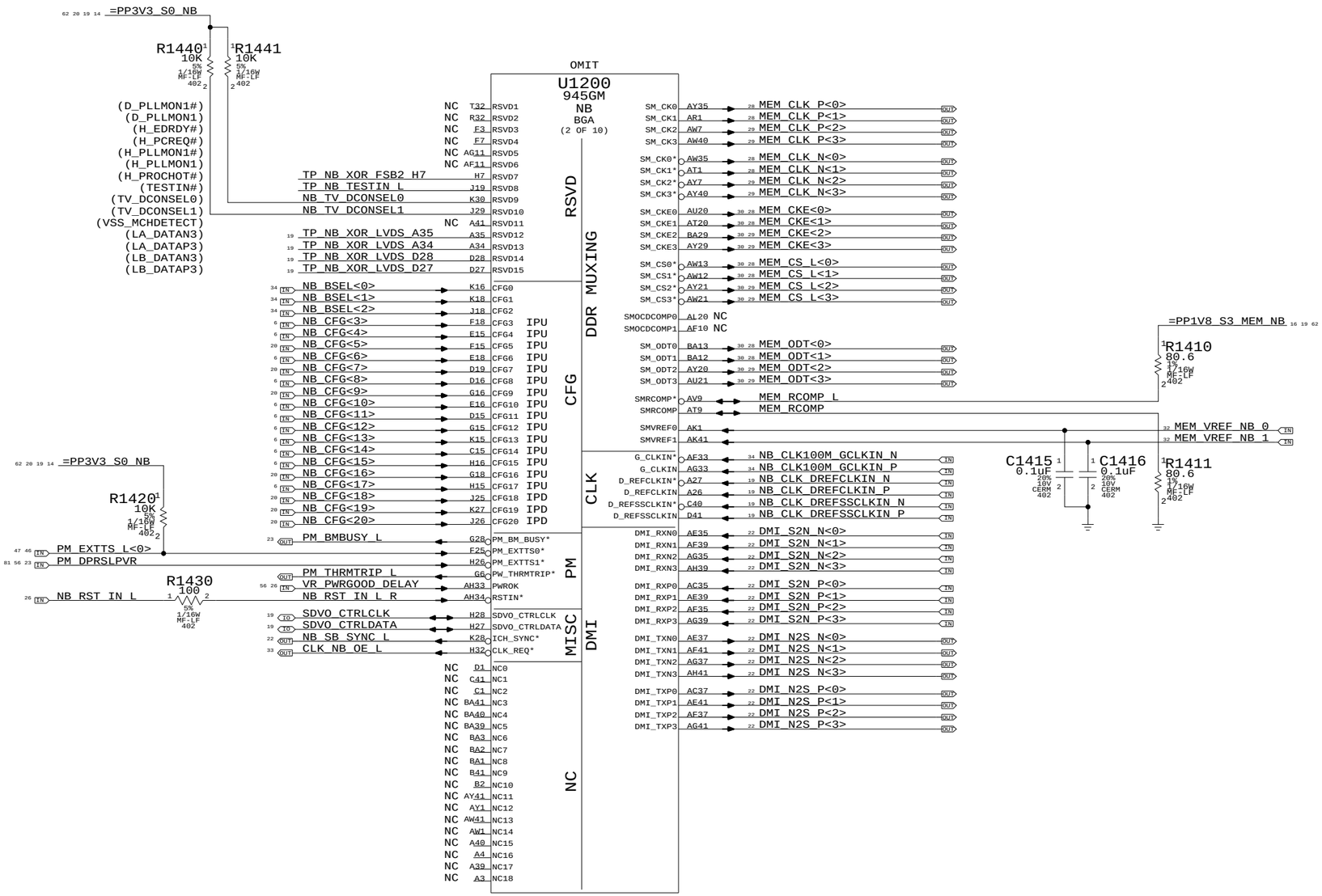

NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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U1200
945GM
NB
BGA
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DDR SYSTEM MEMORY A

MEM_A_DQ<0>	AJ35	SA_DQ0	SA_BS0	AU12	MEM_A_BS<0>
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MEM_A_DQ<4>	AJ36	SA_DQ4	SA_CAS*	AY13	MEM_A_CAS_L
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MEM_A_DQ<52>	AV2	SA_DQ52			
MEM_A_DQ<53>	AT3	SA_DQ53			
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MEM_A_DQ<55>	AL2	SA_DQ55			
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MEM_A_DQ<57>	AF9	SA_DQ57			
MEM_A_DQ<58>	AG4	SA_DQ58			
MEM_A_DQ<59>	AF6	SA_DQ59			
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MEM_A_DQ<61>	AH6	SA_DQ61			
MEM_A_DQ<62>	AF4	SA_DQ62			
MEM_A_DQ<63>	AF8	SA_DQ63			

OMIT

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945GM
NB
BGA
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DDR SYSTEM MEMORY B

MEM_B_DQ<0>	AK39	SB_DQ0	SB_BS0	AT24	MEM_B_BS<0>
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MEM_B_DQ<2>	AP39	SB_DQ2	SB_BS2	AY28	MEM_B_BS<2>
MEM_B_DQ<3>	AR41	SB_DQ3			
MEM_B_DQ<4>	AJ38	SB_DQ4	SB_CAS*	AR24	MEM_B_CAS_L
MEM_B_DQ<5>	AK38	SB_DQ5	SB_DM0	AK36	MEM_B_DM<0>
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MEM_B_DQ<21>	AU36	SB_DQ21	SB_DQS7	AN5	MEM_B_DQS_P<7>
MEM_B_DQ<22>	AP35	SB_DQ22	SB_DQS0*	AM40	MEM_B_DQS_N<0>
MEM_B_DQ<23>	AP34	SB_DQ23	SB_DQS1*	AU39	MEM_B_DQS_N<1>
MEM_B_DQ<24>	AY33	SB_DQ24	SB_DQS2*	AT35	MEM_B_DQS_N<2>
MEM_B_DQ<25>	BA33	SB_DQ25	SB_DQS3*	AP29	MEM_B_DQS_N<3>
MEM_B_DQ<26>	AT31	SB_DQ26	SB_DQS4*	AP16	MEM_B_DQS_N<4>
MEM_B_DQ<27>	AU29	SB_DQ27	SB_DQS5*	AT10	MEM_B_DQS_N<5>
MEM_B_DQ<28>	AU31	SB_DQ28	SB_DQS6*	AT7	MEM_B_DQS_N<6>
MEM_B_DQ<29>	AW31	SB_DQ29	SB_DQS7*	AP5	MEM_B_DQS_N<7>
MEM_B_DQ<30>	AV29	SB_DQ30			
MEM_B_DQ<31>	AW29	SB_DQ31	SB_MA0	AY23	MEM_B_A<0>
MEM_B_DQ<32>	AM19	SB_DQ32	SB_MA1	AW24	MEM_B_A<1>
MEM_B_DQ<33>	AL19	SB_DQ33	SB_MA2	AY24	MEM_B_A<2>
MEM_B_DQ<34>	AP14	SB_DQ34	SB_MA3	AR28	MEM_B_A<3>
MEM_B_DQ<35>	AN14	SB_DQ35	SB_MA4	AT27	MEM_B_A<4>
MEM_B_DQ<36>	AN17	SB_DQ36	SB_MA5	AT28	MEM_B_A<5>
MEM_B_DQ<37>	AM16	SB_DQ37	SB_MA6	AU27	MEM_B_A<6>
MEM_B_DQ<38>	AP15	SB_DQ38	SB_MA7	AV28	MEM_B_A<7>
MEM_B_DQ<39>	AL15	SB_DQ39	SB_MA8	AV27	MEM_B_A<8>
MEM_B_DQ<40>	AJ11	SB_DQ40	SB_MA9	AW27	MEM_B_A<9>
MEM_B_DQ<41>	AH10	SB_DQ41	SB_MA10	AV24	MEM_B_A<10>
MEM_B_DQ<42>	AJ9	SB_DQ42	SB_MA11	BA27	MEM_B_A<11>
MEM_B_DQ<43>	AN10	SB_DQ43	SB_MA12	AY27	MEM_B_A<12>
MEM_B_DQ<44>	AK13	SB_DQ44	SB_MA13	AR23	MEM_B_A<13>
MEM_B_DQ<45>	AH11	SB_DQ45			
MEM_B_DQ<46>	AK10	SB_DQ46	SB_RAS*	AU23	MEM_B_RAS_L
MEM_B_DQ<47>	AJ8	SB_DQ47	SB_RCVENIN*	AK16	NC
MEM_B_DQ<48>	BA10	SB_DQ48	SB_RCVENOUT*	AK18	NC
MEM_B_DQ<49>	AW10	SB_DQ49	SB_WE*	AR27	MEM_B_WE_L
MEM_B_DQ<50>	BA4	SB_DQ50			
MEM_B_DQ<51>	AW4	SB_DQ51			
MEM_B_DQ<52>	AY10	SB_DQ52			
MEM_B_DQ<53>	AY9	SB_DQ53			
MEM_B_DQ<54>	AW5	SB_DQ54			
MEM_B_DQ<55>	AY5	SB_DQ55			
MEM_B_DQ<56>	AV4	SB_DQ56			
MEM_B_DQ<57>	AR5	SB_DQ57			
MEM_B_DQ<58>	AK4	SB_DQ58			
MEM_B_DQ<59>	AK3	SB_DQ59			
MEM_B_DQ<60>	AT4	SB_DQ60			
MEM_B_DQ<61>	AK5	SB_DQ61			
MEM_B_DQ<62>	AJ5	SB_DQ62			
MEM_B_DQ<63>	AJ3	SB_DQ63			

NB DDR2 Interfaces

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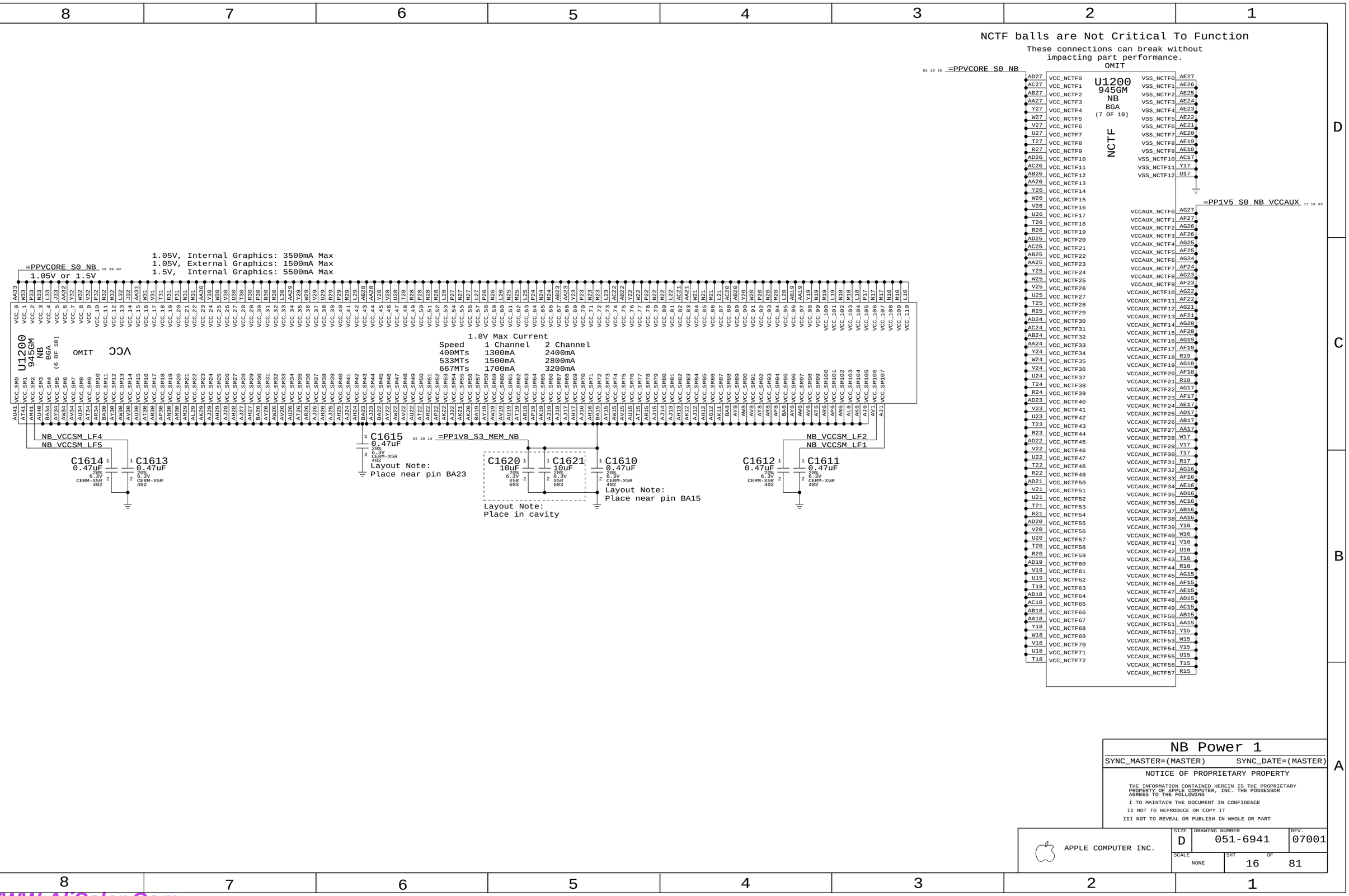

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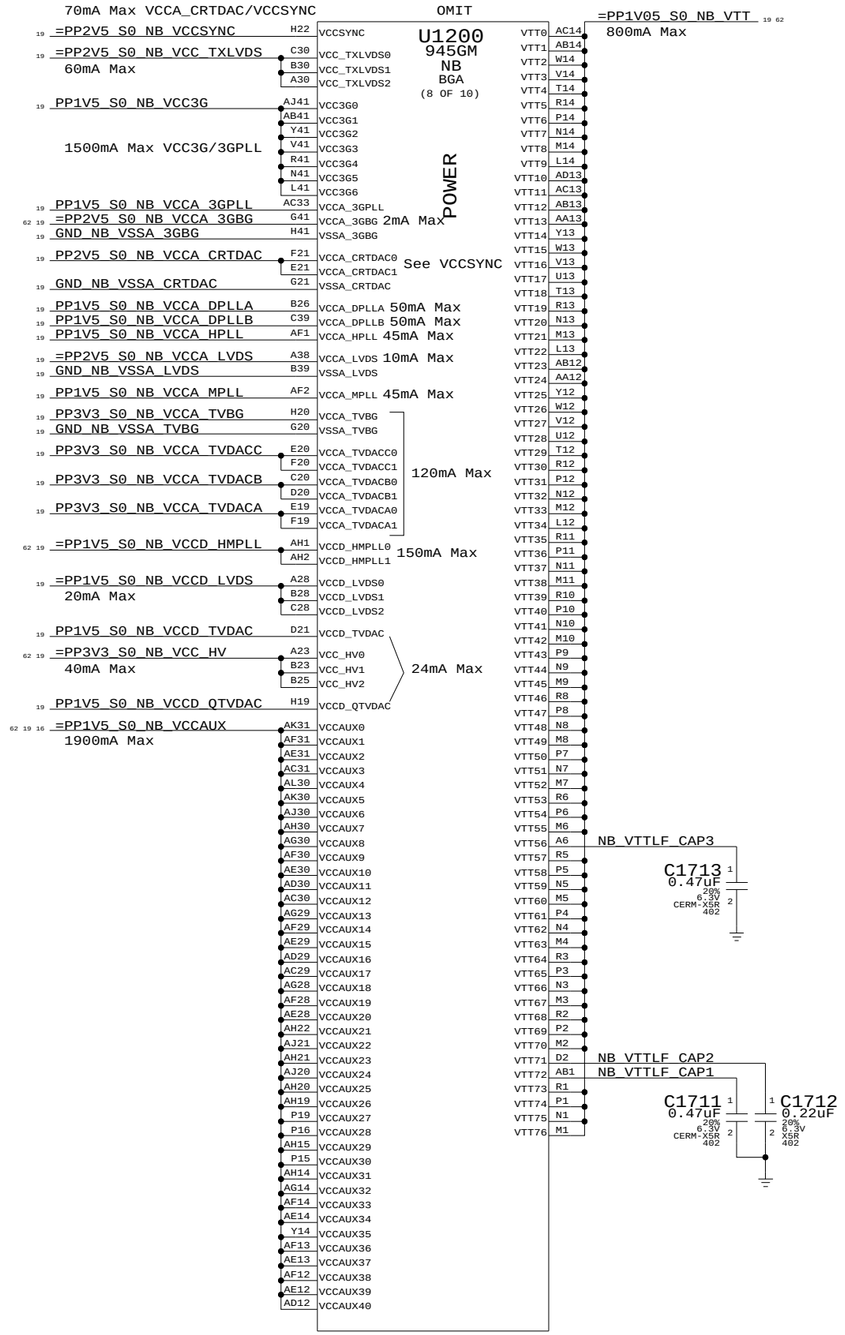

NB Power 2

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VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

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VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

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Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	16 19 62	1500mA Max
	=PP1V05_S0_FSB_NB	12 34 62	10mA Max?
	=PP1V05_S0_NB_VTT	17 19 62	800mA Max
	=PP1V05_S0_NB_CRT	19 62	?mA Max
3674mA Max	=PP1V5_S0_NB	62	?mA Max
	=PP1V5_S0_NB_3G	19 62	1500mA Max
	=PP1V5_S0_NB_3GPLL	19 62	
	=PP1V5_S0_NB_PCIE	13 62	?mA Max
	=PP1V5_S0_NB_PLL	19 62	100mA Max
	=PP1V5_S0_NB_TVDAC	19 62	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	17 62	150mA Max
	=PP1V5_S0_NB_VCCAUX	16 17 19 62	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	14 16 62	3200mA Max
	=PP2V5_S0_NB_VCCSYNC	17 19	70mA Max
132mA Max	=PP2V5_S0_NB_VCC_TXLVDS	17 19	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	17 19 62	2mA Max
	=PP3V3_S0_NB	14 20 62	?mA Max
40mA Max?	=PP3V3_S0_NB_VCC_HV	17 19 62	40mA Max

62 19 =PP1V05_S0_NB_CRT
- CRT_RED — 13
- CRT_GREEN — 13
- CRT_BLUE — 13
- CRT_RED_L — 13
- CRT_GREEN_L — 13
- CRT_BLUE_L — 13
- CRT_IREF — 13
- CRT_HSYNC_R — 13
- CRT_VSYNC_R — 13

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK — 13
TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA — 13

62 19 =PP1V5_S0_NB_TVDAC
- TV_DACA_OUT — 13
- TV_DACB_OUT — 13
- TV_DACC_OUT — 13
- TV_IREF — 13
- TV_IRTNA — 13
- TV_IRTNB — 13
- TV_IRTNC — 13

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL — 13
TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN — 13
TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA — 13
TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB — 13
TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK — 13
TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA — 13
NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG — 13
TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN — 13
NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH — 13
TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL — 13
NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P — 13
NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N — 13
NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0> — 13
NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0> — 13
NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P — 13
NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N — 13
NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0> — 13
NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0> — 13
NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 — 14
NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 — 14
NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 — 14
NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 — 14
TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK — 14
TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA — 14

(MCH LVDS DATA/CLK TX 2.5V PWR) =PP2V5_S0_NB_VCC_TXLVDS — 17 19
(MCH LVDS DIGITAL 1.5V PWR) =PP1V5_S0_NB_VCCD_LVDS — 17
(MCH LVDS ANALOG 2.5V PWR) =PP2V5_S0_NB_VCCA_LVDS — 17

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS — 17

62 19 16 =PPVCORE_S0_NB
- (MCH CRTDAC ANALOG 2.5V PWR) PP2V5_S0_NB_VCCA_CRTDAC — 17
- GND_NB_VSSA_CRTDAC — 17
- (MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC — 17 19

62 19 =PP1V5_S0_NB_TVDAC
- (MCH TV OUT CHANNEL A 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACA — 17
- (MCH TV OUT CHANNEL B 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACB — 17
- (MCH TV OUT CHANNEL C 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACC — 17
- (MCH TV DAC BAND GAP 3.3V PWR) PP3V3_S0_NB_VCCA_TVBG — 17
- GND_NB_VSSA_TVBG — 17

(MCH DISPLAY A PLL 1.5V PWR)
TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA — 17
(MCH DISPLAY B PLL 1.5V PWR)
TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB — 17

- NB_CLK_DREFCLKIN_P — 14
- NB_CLK_DREFCLKIN_N — 14
- NB_CLK_DREFSSCLKIN_P — 14
- NB_CLK_DREFSSCLKIN_N — 14

62 19 16 =PPVCORE_S0_NB, 1500mA Max — GMCH CORE PWR 1.05V BYPASS
C1900 470uF-7MOHM 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V X5R 402
C1905 0.22uF 10% 6.3V X5R 402
C1906 0.22uF 10% 6.3V X5R 402
C1907 0.22uF 10% 6.3V X5R 402

62 19 17 =PP1V05_S0_NB_VTT, 800mA Max — MCH VTT BYPASS (MCH FSB 1.05V PWR)
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note: Place in cavity
(SHARE C0940 470UF)
C1967 0.22uF 20% 6.3V X5R 402
Layout Note: Place on the edge

62 19 17 =PP3V3_S0_NB_VCC_HV, 40mA Max — MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

62 19 17 =PP2V5_S0_NB_VCCA_3GBG, 2mA Max — MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)
C1916 0.1uF 20% 10V CERM 402

62 19 17 16 =PP1V5_S0_NB_VCCAUX, 1900mA Max — GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)
C1918 0.1uF 20% 10V CERM 402

62 19 =PP1V5_S0_NB_TVDAC, 24mA Max
C1921 22000pF-1000mA 10V NPM18 — GMCH VCCD_TVDAC FILTER (MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0_NB_VCCD_TVDAC — 17
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
24mA Max TVDAC/QTVDAC
C1920 0.1uF 20% 10V CERM 402
Layout Note: These 4 caps should be within 6.35 mm of NB edge
C1923 22000pF-1000mA 10V NPM18 — GMCH VCCD_QTVDAC FILTER (MCH TVDAC DIGITAL QUIET 1.5V PWR) PP1V5_S0_NB_VCCD_QTVDAC — 17
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
L1922 180-OHM-1.5A 0603 — PP1V5_S0_NB_QTVDAC
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
C1922 0.1uF 20% 10V CERM 402

62 19 =PP1V5_S0_NB_3G, 1500mA Max — GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)
L1970 91nH 1210
Layout Note: Place L and C close to MCH
C1970 220UF 20% 2.5V POLY SMB2
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.
PP1V5_S0_NB_VCC3G — 17
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
1500mA Max

62 19 =PP1V5_S0_NB_3GPLL, 1500mA Max — GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)
L1975 1.0UH-220MA-0.12-OHM 0805 — PP1V5_S0_NB_3GPLL_F
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=1.5V
R1975 0.51 1% 1/10W MF-LF 402
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
Layout Note: 3GPLL 10uF cap should be placed in cavity
PP1V5_S0_NB_VCCA_3GPLL — 17
MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
GND_NB_VSSA_3GBG — 17
Layout Note: Route to caps, then GND

62 19 =PP1V5_S0_NB_PLL, 100mA Max — GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR)
L1934 FERR-120-OHM-0.2A 0603 — PP1V5_S0_NB_VCCA_HPLL — 17
MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
45mA Max
C1934 22uF 20% 6.3V X5R 805
C1935 0.1uF 20% 10V CERM 402
GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR)
L1936 FERR-120-OHM-0.2A 0603 — PP1V5_S0_NB_VCCA_MPLL — 17
MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
45mA Max
C1936 22uF 20% 6.3V X5R 805
C1937 0.1uF 20% 10V CERM 402

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE: NONE	SHT 19 OF 81	

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NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 62
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 62
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 62
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	20	81

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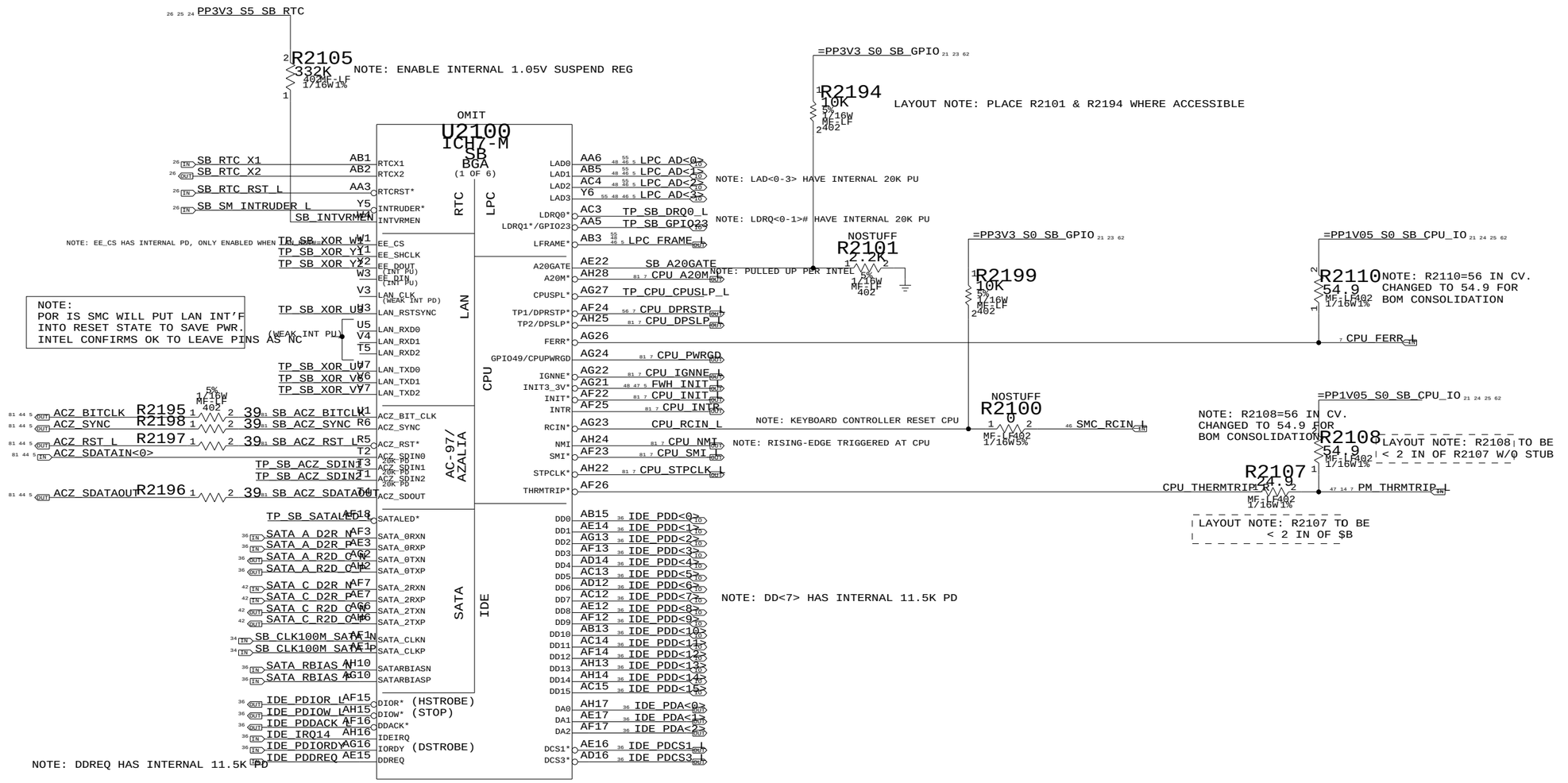

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

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NONE	21	81

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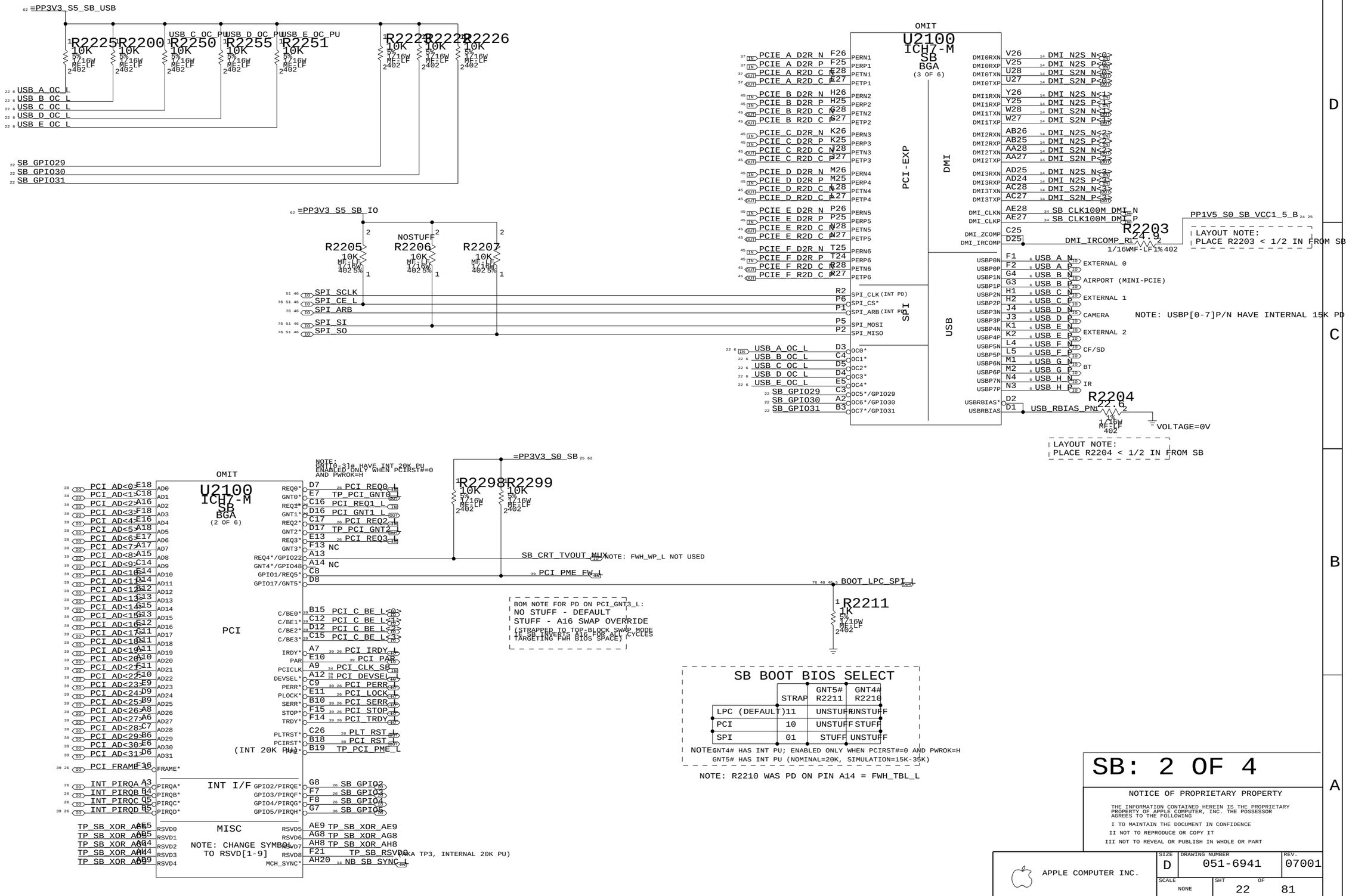

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NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 62

=PP3V3_S5_SB 23 25 62

NO_REBOOT_MODE

RP2300 10K 5% 1/16W 8M-LF

R2318 10K 1/16W 402 2MF-LF 5%
R2395 8.2K 1/16W 402 2MF-LF 5%
R2396 10K 1/16W 402 2MF-LF 5%
R2397 8.2K 1/16W 402 2MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2323 1K 1/16W 402 2MF-LF 5%

62 25 23 =PP3V3_S5_SB

R2398 1K 1/16W 402 2MF-LF 5%
R2320 10K 1/16W 402 2MF-LF 5%
R2317 10K 1/16W 402 2MF-LF 5%
R2316 10K 1/16W 402 2MF-LF 5%

OMIT
U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB_CLK 27 (IO) — C22 SMBCLK
SMB_DATA 27 (IO) — B22 SMBDATA
SMB_LINK_ALERT_L — A16 SMLINKALERT*
SMLINK<0> — B25 SMLINK0
NOT USED — SMLINK<1> — A25 SMLINK1

SMB

PM_RI_L — A28 RI*

SB_SPKR — A19 SPKR (INT WEAK PD)

PM_SUS_STAT_L 55 48 46 5 (OUT) — A27 SUS_STAT*
PM_SYSRST_L 46 26 (IN) — A22 SYS_RST*

CLKS

PM_BMBUSY_L 14 (IN) — AB18 GPIO0/BM_BUSY*

SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE

PM_STPPCI_L 33 (OUT) — AC20 GPIO18/STPPCI*
PM_STPCPU_L 33 (OUT) — AF21 GPIO20/STPCPU*

SB_GPIO26 — A21 GPIO26

BIOS_REC 23 — B21 GPIO27
FWH_MFG_MODE 23 — E23 GPIO28

PM_CLKRUN_L 55 48 46 39 5 (IO) — AG18 GPIO32/CLKRUN*

RESERVED FOR MOBILE AZALIA DOCKING INTF
TP_AZ_DOCK_EN — AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST — U2 GPIO34/AZ_DOCK_RST*

PCIE_WAKE_L 44 37 5 (IN) — F20 WAKE*
INT_SERIRQ 55 48 46 5 (IO) — AH21 SERIRQ
PM_THRM_L 46 (IN) — AF20 THRM*

VR_PWRGD_CK410 26 (IN) — AD22 VRMPWRGD

TP_SB_GPIO6 (IO) — AG21 GPIO6
SB_RUNTIME_SCI_L — AC18 GPIO7
E21 GPIO8

SYS GPIO

PWR MNGT

SATA GPIO

GPIO21/SATA0GP — AF19 SB_GPIO21 100 1 2 R2302
GPIO19/SATA1GP — AH18 SB_GPIO19 100 1 2 R2303
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19 SB_GPIO37 100 1 2 R2305

36 SATA_C_DET_L (IN)

CLK14 — AC1 34 SB_CLK14P3M_TIMER (IN)
CLK48 — B2 34 SB_CLK48M_USBC_LR (IN)
SUSCLK — C20 8 SUS_CLK_SB (OUT)

SLP_S3* — B24 64 46 PM_SLP_S3_L (OUT)
SLP_S4* — D23 64 46 PM_SLP_S4_L (OUT)
SLP_S5* — F22 46 PM_SLP_S5_L (OUT)
PWROK — AA4 26 PM_SB_PWROK (IN)
GPIO16/DPRSLPVR — AC22 81 56 14 PM_DPRSLPVR (OUT)
TP0/BATLOW* — C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
PWRBTN* (INT 20K PU) — C23 46 PM_PWRBTN_L (IN)
LAN_RST* — C19 46 PM_LAN_ENABLE (IN) NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4

GPIO9 — E20 47 46 SMS_INT_L (IN)
GPIO10 — A20 46 SMC_SB_NMI (IN)
DEF=GPI GPIO12 — F19 23 PATA_PWR_EN_L (OUT)
GPIO13 — E19
DEF=GPI GPIO14 — R4 36 IDE_RESET_L (OUT)
GPIO15 — E22 SV_SET_UP 5 23 48
GPIO24 — R3 CRB_SV_DET 23
GPIO25 — D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 33 SB_CLK100M_SATA_OE_L (OUT)
GPIO38 — AD20 TP_SB_GPIO38 (IO)
DEF=GPI GPIO39 — AE20 23 SATA_C_PWR_EN_L (OUT)

GPIO

=PP3V3_S5_SB_PM 11 26 62

R2319 10K 1/16W 402 2MF-LF 5%
R2343 8.2K 1/16W 402 2MF-LF 5%

46 PM_BATLOW_L (IN)

R2399 100K 1/16W 402 2MF-LF 5%

46 PM_RSMRST_L (IN)

46 SMC_WAKE_SCI_L (IN)

NOSTUFF
R2300 0

46 SMC_RUNTIME_SCI_L 1 2 (IN)
46 SMC_EXTSMI_L (IN)

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

62 25 23 =PP3V3_S5_SB

NOSTUFF R2306 10K 1/16W 402 2MF-LF 5%
R2308 10K 1/16W 402 2MF-LF 5%

SV_SET_UP 5 23 48
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 402 2MF-LF 5%
NOSTUFF R2309 0 1/16W 402 2MF-LF 5%

62 25 23 =PP3V3_S5_SB

R2313 10K 1/16W 402 2MF-LF 5%
R2310 10K 1/16W 402 2MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

NOSTUFF R2314 0 1/16W 402 2MF-LF 5%
NOSTUFF R2311 10K 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 23 25 62

R2390 10K 5% 1/16W 2MF-LF 402

23 PATA_PWR_EN_L

=PP3V3_S0_SB_GPIO 21 23 62

R2388 10K 5% 1/16W 2MF-LF 402

23 SATA_C_PWR_EN_L

SB: 3 OF 4

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NONE	23	81

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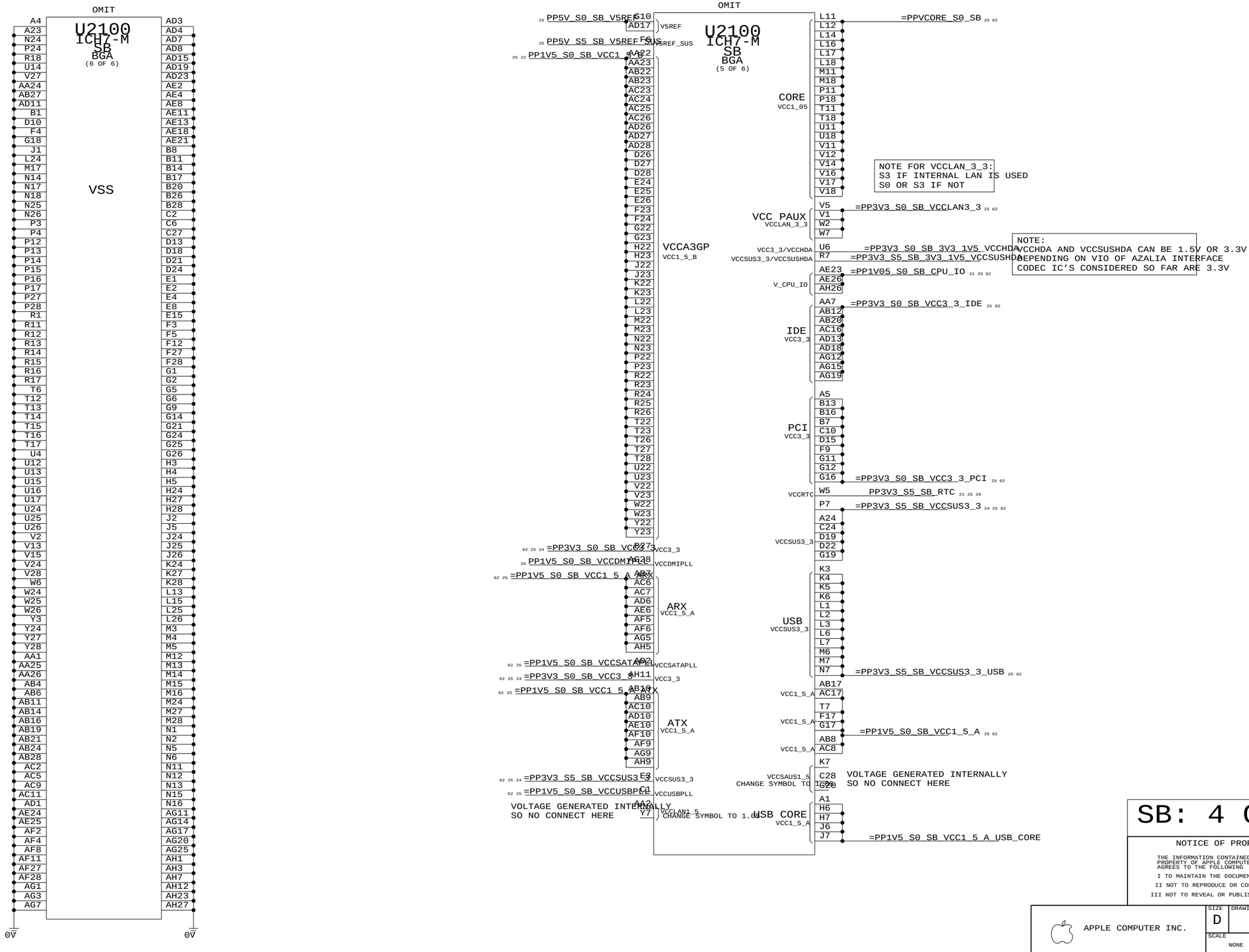

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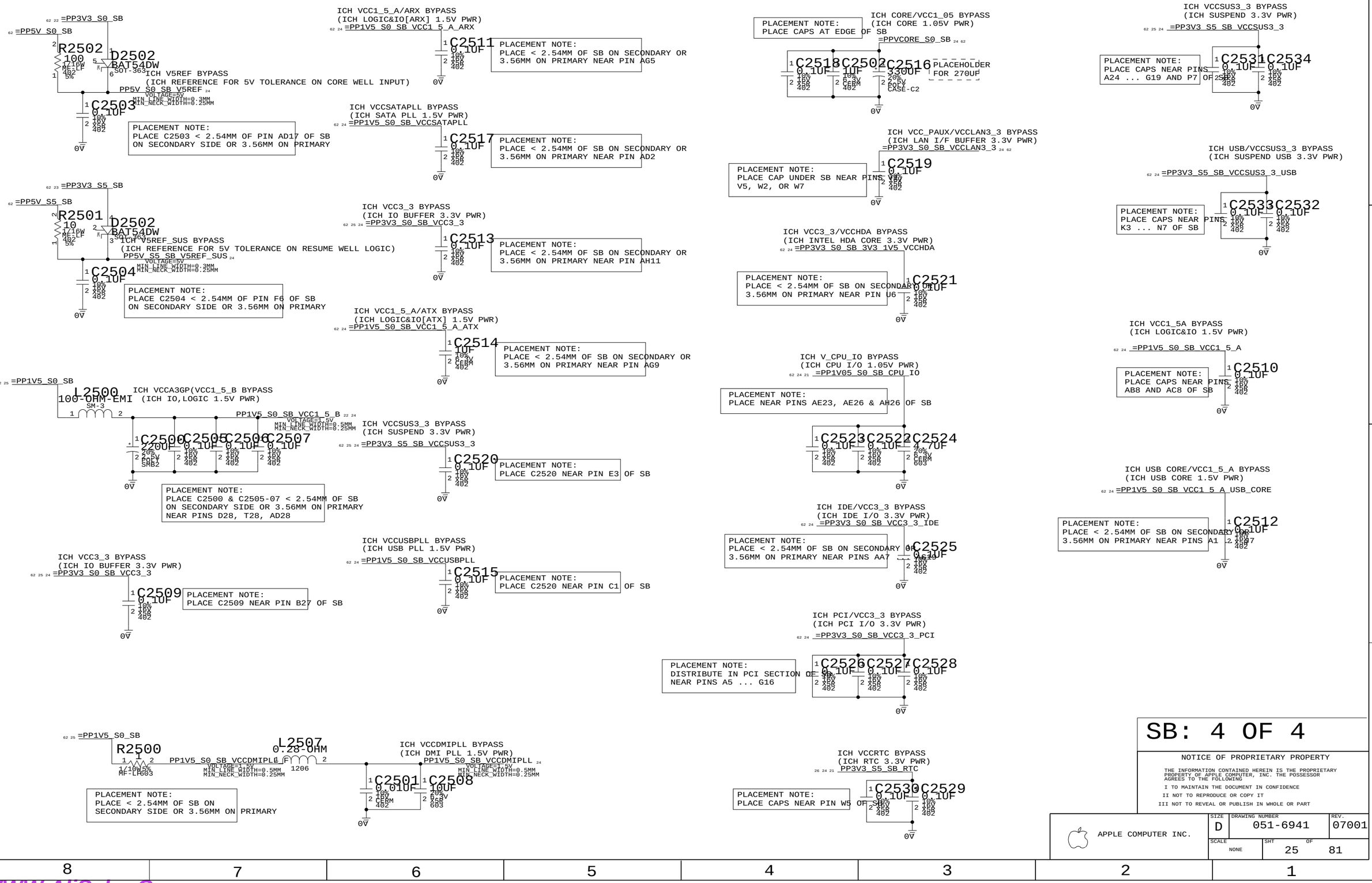

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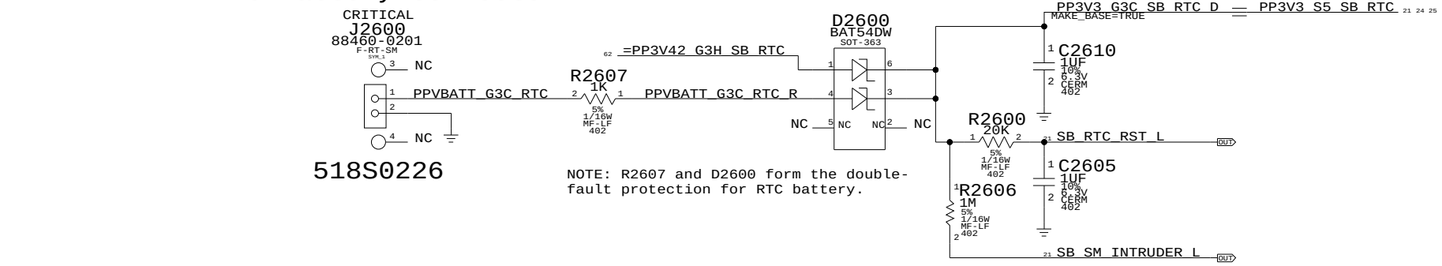
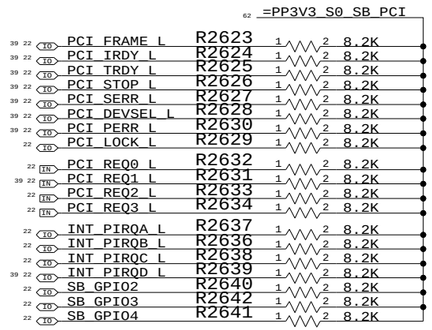
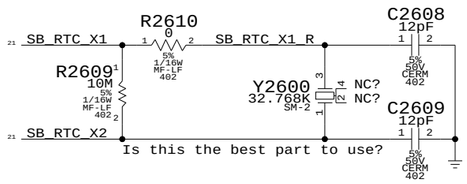
RTC Battery Connector



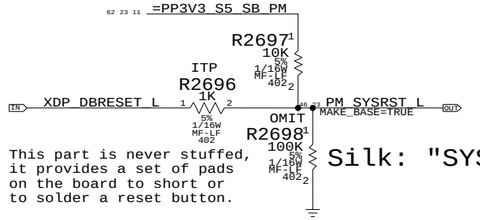
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



Is this the best part to use?

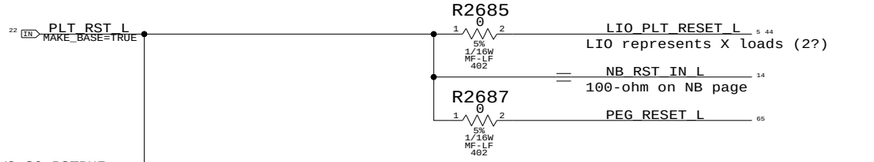


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

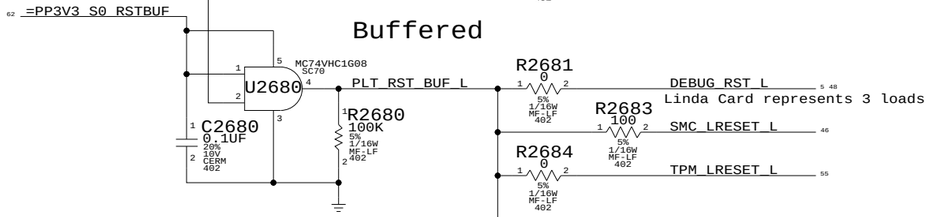
Silk: "SYS RST"

Platform Reset Connections

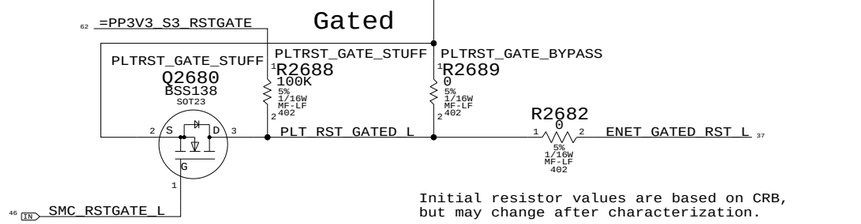
Unbuffered



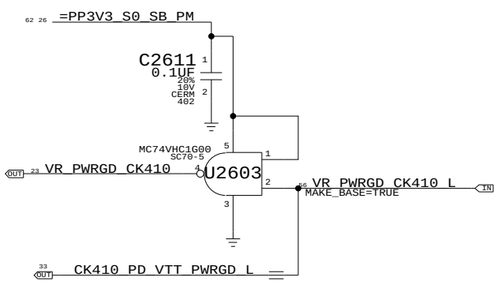
Buffered



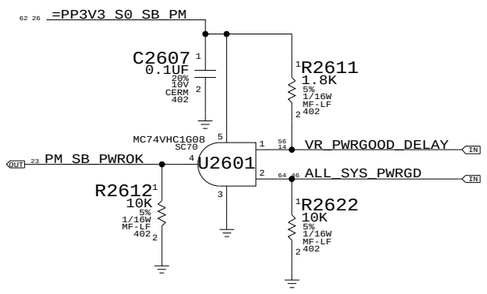
Gated



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	26	81

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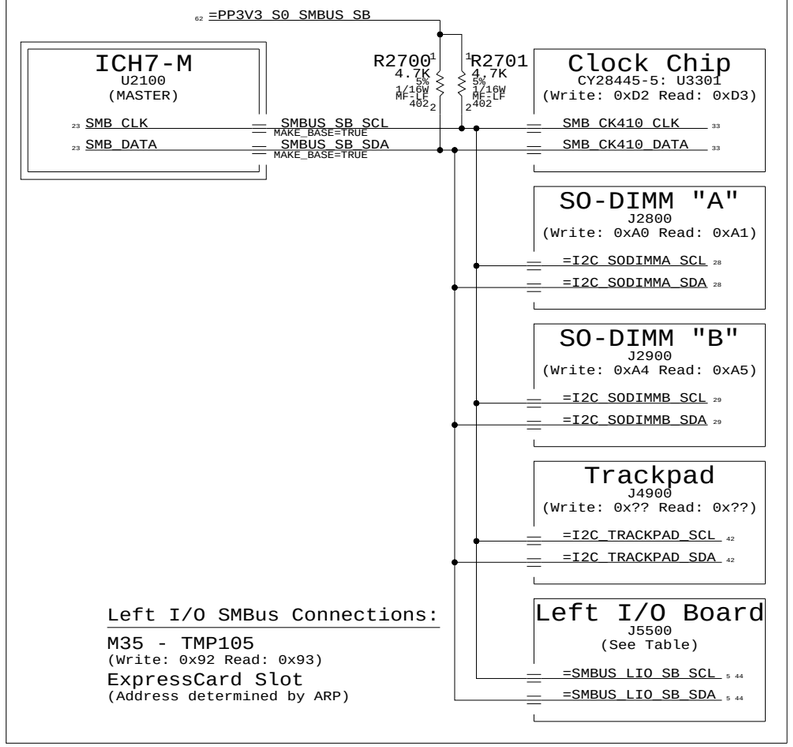
ICH7-M SMBus Connections

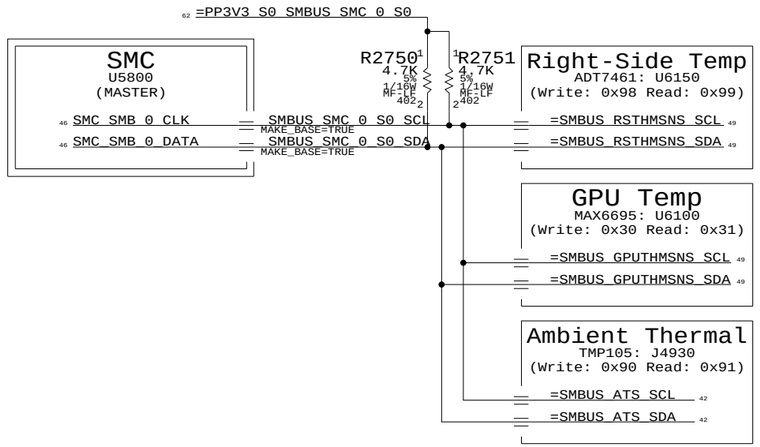


Left I/O SMBus Connections:

M35 - TMP105
(Write: 0x92 Read: 0x93)

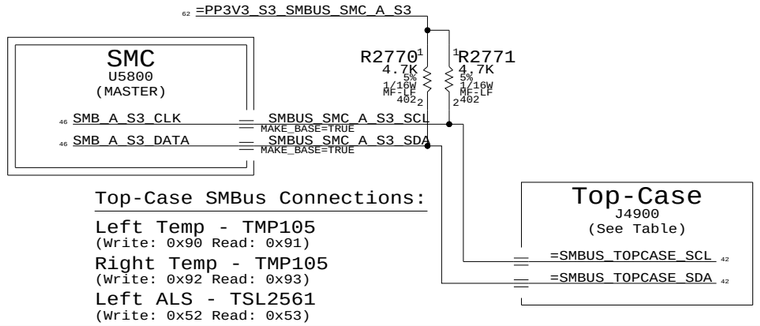
ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections



SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



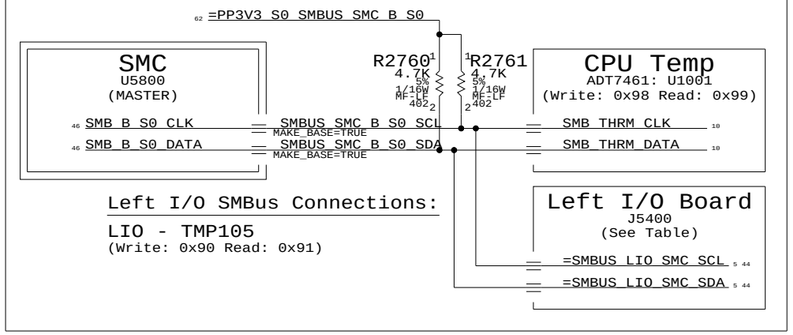
Top-Case SMBus Connections:

Left Temp - TMP105
(Write: 0x90 Read: 0x91)

Right Temp - TMP105
(Write: 0x92 Read: 0x93)

Left ALS - TSL2561
(Write: 0x52 Read: 0x53)

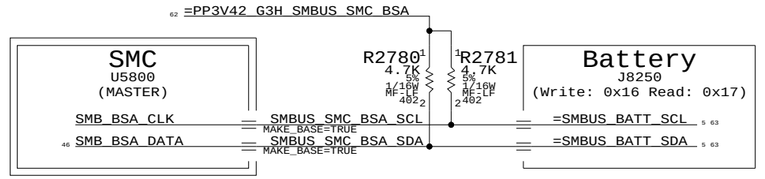
SMC "B" SMBus Connections



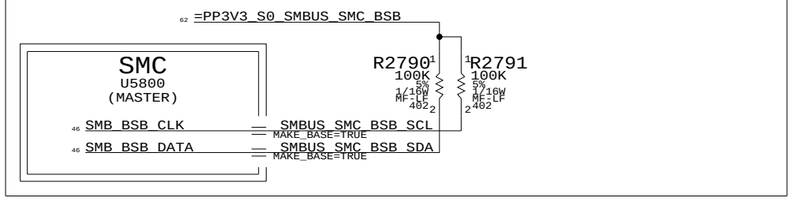
Left I/O SMBus Connections:

LIO - TMP105
(Write: 0x90 Read: 0x91)

SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	27	81

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Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (surface-mount) slot

62 29 28 =PP1V8_S3_MEM
32 29 MEM_VREF
C2800 0.1uF 20% 10V CERM 402

J2800 F-RT-SM DDR2-SODIMM-DUAL

203 NC
201 NC

	1A	VREF		VSS0	2A		
	3A	VSS1		DQ4	4A	MEM_A_DQ<8>	15
15	5A	DQ0	15	DQ5	6A	MEM_A_DQ<12>	15
15	7A	DQ1		VSS2	8A		
	9A	VSS4		DM0	10A	MEM_A_DM<1>	15
15	11A	DQS0*		VSS5	12A		
15	13A	DQS0	15	DQ6	14A	MEM_A_DQ<15>	15
	15A	VSS6	15	DQ7	16A	MEM_A_DQ<9>	15
15	17A	DQ2		VSS7	18A		
15	19A	DQ3	15	DQ12	20A	MEM_A_DQ<2>	15
	21A	VSS8	15	DQ13	22A	MEM_A_DQ<3>	15
15	23A	DQ8		VSS9	24A		
15	25A	DQ9		DM1	26A	MEM_A_DM<0>	15
	27A	VSS10		VSS11	28A		
15	29A	DQS1*	14	CK0	30A	MEM_CLK_P<0>	14
15	31A	DQS1	14	CK0*	32A	MEM_CLK_N<0>	14
	33A	VSS12		VSS13	34A		
15	35A	DQ10	15	DQ14	36A	MEM_A_DQ<1>	15
15	37A	DQ11	15	DQ15	38A	MEM_A_DQ<0>	15
	39A	VSS14		VSS15	40A		
		KEY					
	41A	VSS16		VSS17	42A		
15	43A	DQ16	15	DQ20	44A	MEM_A_DQ<23>	15
15	45A	DQ17	15	DQ21	46A	MEM_A_DQ<22>	15
	47A	VSS18		VSS19	48A		
15	49A	DQS2*		NC0	50A	DIMM_OVERTEMP_L	29 47
15	51A	DQS2	15	DM2	52A	MEM_A_DM<2>	15
	53A	VSS21		VSS22	54A		
15	55A	DQ18	15	DQ22	56A	MEM_A_DQ<21>	15
15	57A	DQ19	15	DQ23	58A	MEM_A_DQ<17>	15
	59A	VSS23		VSS24	60A		
15	61A	DQ24	15	DQ28	62A	MEM_A_DQ<29>	15
15	63A	DQ25	15	DQ29	64A	MEM_A_DQ<24>	15
	65A	VSS25		VSS26	66A		
15	67A	DM3	15	DQS3*	68A	MEM_A_DQS_N<3>	15
NC	69A	NC1	15	DQS3	70A	MEM_A_DQS_P<3>	15
	71A	VSS27		VSS28	72A		
15	73A	DQ26	15	DQ30	74A	MEM_A_DQ<26>	15
15	75A	DQ27	15	DQ31	76A	MEM_A_DQ<31>	15
	77A	VSS29		VSS30	78A		
30 14	79A	CKE0		NC/CKE1	80A	MEM_CKE<1>	14 30
	81A	VDD0		VDD1	82A		
NC	83A	NC2		NC/A15	84A	MEM_A_A<15>	6
30 15	85A	BA2		NC/A14	86A	MEM_A_A<14>	6
	87A	VDD2		VDD3	88A		
30 15	89A	A12	30	A11	90A	MEM_A_A<11>	15 30
30 15	91A	A9	30	A7	92A	MEM_A_A<7>	15 30
30 15	93A	A8	30	A6	94A	MEM_A_A<6>	15 30
	95A	VDD4		VDD5	96A		
30 15	97A	A5	30	A4	98A	MEM_A_A<4>	15 30
30 15	99A	A3	30	A2	100A	MEM_A_A<2>	15 30
30 15	101A	A1	30	A0	102A	MEM_A_A<0>	15 30
	103A	VDD6		VDD7	104A		
30 15	105A	A10/AP	30	BA1	106A	MEM_A_BS<1>	15 30
30 15	107A	BA0	30	RAS*	108A	MEM_A_RAS_L	15 30
30 15	109A	WE*	30	S0*	110A	MEM_CS_L<0>	14 30
	111A	VDD8		VDD9	112A		
30 15	113A	CAS*	30	ODT0	114A	MEM_ODT<0>	14 30
30 14	115A	NC/S1*		NC/A13	116A	MEM_A_A<13>	15 30
	117A	VDD10		VDD11	118A		
30 14	119A	NC/ODT1		NC3	120A	NC	
	121A	VSS31		VSS32	122A		
15	123A	DQ32	15	DQ36	124A	MEM_A_DQ<38>	15
15	125A	DQ33	15	DQ37	126A	MEM_A_DQ<34>	15
	127A	VSS33		VSS34	128A		
15	129A	DQS4*		DM4	130A	MEM_A_DM<4>	15
15	131A	DQS4		VSS35	132A		
	133A	VSS36	15	DQ38	134A	MEM_A_DQ<32>	15
15	135A	DQ34	15	DQ39	136A	MEM_A_DQ<36>	15
15	137A	DQ35		VSS37	138A		
	139A	VSS38	15	DQ44	140A	MEM_A_DQ<57>	15
15	141A	DQ40	15	DQ45	142A	MEM_A_DQ<63>	15
15	143A	DQ41		VSS39	144A		
	145A	VSS40	15	DQS5*	146A	MEM_A_DQS_N<7>	15
15	147A	DM5	15	DQS5	148A	MEM_A_DQS_P<7>	15
	149A	VSS41		VSS42	150A		
15	151A	DQ42	15	DQ46	152A	MEM_A_DQ<56>	15
15	153A	DQ43	15	DQ47	154A	MEM_A_DQ<62>	15
	155A	VSS43		VSS44	156A		
15	157A	DQ48	15	DQ52	158A	MEM_A_DQ<40>	15
15	159A	DQ49	15	DQ53	160A	MEM_A_DQ<42>	15
	161A	VSS45		VSS46	162A		
NC	163A	NC_TEST	14	CK1	164A	MEM_CLK_P<1>	14
	165A	VSS47	14	CK1*	166A	MEM_CLK_N<1>	14
15	167A	DQS6*		VSS48	168A		
15	169A	DQS6	15	DM6	170A	MEM_A_DM<5>	15
	171A	VSS49		VSS50	172A		
15	173A	DQ50	15	DQ54	174A	MEM_A_DQ<47>	15
15	175A	DQ51	15	DQ55	176A	MEM_A_DQ<44>	15
	177A	VSS51		VSS52	178A		
15	179A	DQ56	15	DQ60	180A	MEM_A_DQ<54>	15
15	181A	DQ57	15	DQ61	182A	MEM_A_DQ<55>	15
	183A	VSS53		VSS54	184A		
15	185A	DM7	15	DQS7*	186A	MEM_A_DQS_N<6>	15
	187A	VSS55	15	DQS7	188A	MEM_A_DQS_P<6>	15
15	189A	DQ58		VSS56	190A		
15	191A	DQ59	15	DQ62	192A	MEM_A_DQ<52>	15
62 29	193A	VSS57	15	DQ63	194A	MEM_A_DQ<49>	15
27	195A	SDA		VSS58	196A		
27	197A	SCL		SA0	198A	ADDR=0xA0(WR)/0xA1(RD)	
	199A	VDDSPD		SA1	200A		

202 NC
204 NC
516S0382

62 29 28 =PPSPD_S0_MEM
27 =I2C_SODIMMA_SDA
27 =I2C_SODIMMA_SCL

62 29 28 =PP1V8_S3_MEM
28 29 62

DDR2 Bypass Caps
(For return current)

62 29 28 =PP1V8_S3_MEM

C2808 10UF 20% 6.3V X5R 603	C2809 10UF 20% 6.3V X5R 603		
C2810 0.1UF 20% 10V CERM 402	C2811 0.1UF 20% 10V CERM 402	C2812 0.1UF 20% 10V CERM 402	C2813 0.1UF 20% 10V CERM 402
C2814 0.1UF 20% 10V CERM 402	C2815 0.1UF 20% 10V CERM 402	C2816 0.1UF 20% 10V CERM 402	C2817 0.1UF 20% 10V CERM 402
C2818 0.1UF 20% 10V CERM 402	C2819 0.1UF 20% 10V CERM 402	C2820 0.1UF 20% 10V CERM 402	C2821 0.1UF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

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D	051-6941	07001
SCALE: NONE	SHT 28 OF 81	

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Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (thru-hole) slot

62 29 28 =PP1V8_S3_MEM
32 28 MEM_VREF
C2900 0.1uF 20% 10V CERM 402

J2900 F-RT-TH DDR2-SODIMM-DUAL

		1B	VREF	VSS0	2B		
		3B	VSS1	DQ4	4B	MEM_B_DQ<9>	15
15	MEM_B_DQ<15>	5B	DQ0	DQ5	6B	MEM_B_DQ<11>	15
15	MEM_B_DQ<14>	7B	DQ1	VSS2	8B		
		9B	VSS4	DM0	10B	MEM_B_DM<1>	15
15	MEM_B_DQS_N<1>	11B	DQS0*	VSS5	12B		
15	MEM_B_DQS_P<1>	13B	DQS0	DQ6	14B	MEM_B_DQ<12>	15
		15B	VSS6	DQ7	16B	MEM_B_DQ<8>	15
15	MEM_B_DQ<10>	17B	DQ2	VSS7	18B		
15	MEM_B_DQ<13>	19B	DQ3	DQ12	20B	MEM_B_DQ<3>	15
		21B	VSS8	DQ13	22B	MEM_B_DQ<6>	15
15	MEM_B_DQ<7>	23B	DQ8	VSS9	24B		
15	MEM_B_DQ<2>	25B	DQ9	DM1	26B	MEM_B_DM<0>	15
		27B	VSS10	VSS11	28B		
15	MEM_B_DQS_N<0>	29B	DQS1*	CK0	30B	MEM_CLK_P<3>	14
15	MEM_B_DQS_P<0>	31B	DQS1	CK0*	32B	MEM_CLK_N<3>	14
		33B	VSS12	VSS13	34B		
15	MEM_B_DQ<1>	35B	DQ10	DQ14	36B	MEM_B_DQ<0>	15
15	MEM_B_DQ<4>	37B	DQ11	DQ15	38B	MEM_B_DQ<5>	15
		39B	VSS14	VSS15	40B		
			KEY				
		41B	VSS16	VSS17	42B		
15	MEM_B_DQ<21>	43B	DQ16	DQ20	44B	MEM_B_DQ<22>	15
15	MEM_B_DQ<19>	45B	DQ17	DQ21	46B	MEM_B_DQ<18>	15
		47B	VSS18	VSS19	48B		
15	MEM_B_DQS_N<2>	49B	DQS2*	NC0	50B	DIMM_OVERTEMP_L	28 47
15	MEM_B_DQS_P<2>	51B	DQS2	DM2	52B	MEM_B_DM<2>	15
		53B	VSS21	VSS22	54B		
15	MEM_B_DQ<20>	55B	DQ18	DQ22	56B	MEM_B_DQ<17>	15
15	MEM_B_DQ<23>	57B	DQ19	DQ23	58B	MEM_B_DQ<16>	15
		59B	VSS23	VSS24	60B		
15	MEM_B_DQ<29>	61B	DQ24	DQ28	62B	MEM_B_DQ<26>	15
15	MEM_B_DQ<24>	63B	DQ25	DQ29	64B	MEM_B_DQ<28>	15
		65B	VSS25	VSS26	66B		
15	MEM_B_DM<3>	67B	DM3	DQS3*	68B	MEM_B_DQS_N<3>	15
	NC	69B	NC1	DQS3	70B	MEM_B_DQS_P<3>	15
		71B	VSS27	VSS28	72B		
15	MEM_B_DQ<27>	73B	DQ26	DQ30	74B	MEM_B_DQ<31>	15
15	MEM_B_DQ<25>	75B	DQ27	DQ31	76B	MEM_B_DQ<30>	15
		77B	VSS29	VSS30	78B		
30 14	MEM_CKE<2>	79B	CKE0	NC/CKE1	80B	MEM_CKE<3>	14 30
		81B	VDD0	VDD1	82B		
	NC	83B	NC2	NC/A15	84B	MEM_B_A<15>	6
30 15	MEM_B_BS<2>	85B	BA2	NC/A14	86B	MEM_B_A<14>	6
		87B	VDD2	VDD3	88B		
30 15	MEM_B_A<12>	89B	A12	A11	90B	MEM_B_A<11>	15 30
30 15	MEM_B_A<9>	91B	A9	A7	92B	MEM_B_A<7>	15 30
30 15	MEM_B_A<8>	93B	A8	A6	94B	MEM_B_A<6>	15 30
		95B	VDD4	VDD5	96B		
30 15	MEM_B_A<5>	97B	A5	A4	98B	MEM_B_A<4>	15 30
30 15	MEM_B_A<3>	99B	A3	A2	100B	MEM_B_A<2>	15 30
30 15	MEM_B_A<1>	101B	A1	A0	102B	MEM_B_A<0>	15 30
		103B	VDD6	VDD7	104B		
30 15	MEM_B_A<10>	105B	A10/AP	BA1	106B	MEM_B_BS<1>	15 30
30 15	MEM_B_BS<0>	107B	BA0	RAS*	108B	MEM_B_RAS_L	15 30
30 15	MEM_B_WE_L	109B	WE*	S0*	110B	MEM_CS_L<2>	14 30
		111B	VDD8	VDD9	112B		
30 15	MEM_B_CAS_L	113B	CAS*	ODT0	114B	MEM_ODT<2>	14 30
30 14	MEM_CS_L<3>	115B	NC/S1*	NC/A13	116B	MEM_B_A<13>	15 30
		117B	VDD10	VDD11	118B		
30 14	MEM_ODT<3>	119B	NC/ODT1	NC3	120B	NC	
		121B	VSS31	VSS32	122B		
15	MEM_B_DQ<36>	123B	DQ32	DQ36	124B	MEM_B_DQ<32>	15
15	MEM_B_DQ<33>	125B	DQ33	DQ37	126B	MEM_B_DQ<37>	15
		127B	VSS33	VSS34	128B		
15	MEM_B_DQS_N<4>	129B	DQS4*	DM4	130B	MEM_B_DM<4>	15
15	MEM_B_DQS_P<4>	131B	DQS4	VSS35	132B		
		133B	VSS36	DQ38	134B	MEM_B_DQ<38>	15
15	MEM_B_DQ<34>	135B	DQ34	DQ39	136B	MEM_B_DQ<39>	15
15	MEM_B_DQ<35>	137B	DQ35	VSS37	138B		
		139B	VSS38	DQ44	140B	MEM_B_DQ<44>	15
15	MEM_B_DQ<40>	141B	DQ40	DQ45	142B	MEM_B_DQ<45>	15
15	MEM_B_DQ<41>	143B	DQ41	VSS39	144B		
		145B	VSS40	DQS5*	146B	MEM_B_DQS_N<5>	15
15	MEM_B_DM<5>	147B	DM5	DQS5	148B	MEM_B_DQS_P<5>	15
		149B	VSS41	VSS42	150B		
15	MEM_B_DQ<42>	151B	DQ42	DQ46	152B	MEM_B_DQ<46>	15
15	MEM_B_DQ<43>	153B	DQ43	DQ47	154B	MEM_B_DQ<47>	15
		155B	VSS43	VSS44	156B		
15	MEM_B_DQ<62>	157B	DQ48	DQ52	158B	MEM_B_DQ<58>	15
15	MEM_B_DQ<59>	159B	DQ49	DQ53	160B	MEM_B_DQ<63>	15
		161B	VSS45	VSS46	162B		
	NC	163B	NC_TEST	CK1	164B	MEM_CLK_P<2>	14
		165B	VSS47	CK1*	166B	MEM_CLK_N<2>	14
15	MEM_B_DQS_N<7>	167B	DQS6*	VSS48	168B		
15	MEM_B_DQS_P<7>	169B	DQS6	DM6	170B	MEM_B_DM<7>	15
		171B	VSS49	VSS50	172B		
15	MEM_B_DQ<60>	173B	DQ50	DQ54	174B	MEM_B_DQ<56>	15
15	MEM_B_DQ<61>	175B	DQ51	DQ55	176B	MEM_B_DQ<57>	15
		177B	VSS51	VSS52	178B		
15	MEM_B_DQ<54>	179B	DQ56	DQ60	180B	MEM_B_DQ<55>	15
15	MEM_B_DQ<51>	181B	DQ57	DQ61	182B	MEM_B_DQ<50>	15
		183B	VSS53	VSS54	184B		
15	MEM_B_DM<6>	185B	DM7	DQS7*	186B	MEM_B_DQS_N<6>	15
		187B	VSS55	DQS7	188B	MEM_B_DQS_P<6>	15
15	MEM_B_DQ<52>	189B	DQ58	VSS56	190B		
15	MEM_B_DQ<49>	191B	DQ59	DQ62	192B	MEM_B_DQ<53>	15
62 29 28	=PPSPD_S0_MEM	193B	VSS57	DQ63	194B	MEM_B_DQ<48>	15
27	=I2C_SODIMMB_SDA	195B	SDA	VSS58	196B		
27	=I2C_SODIMMB_SCL	197B	SCL	SA0	198B		
		199B	VDDSPD	SA1	200B		

20 NC
202 NC
516-0130

=PP1V8_S3_MEM 28 29 62

=PPSPD_S0_MEM 28 29 62
R2900 10K 5% 1/10W MF-LF 402
Resistor prevents pwr-gnd short

SODIMM_A_SA1
ADDR=0xA4(WR)/0xA5(RD)

DDR2 Bypass Caps
(For return current)

62 29 28 =PP1V8_S3_MEM

C2908 10UF 20% 6.3V X5R 603
C2909 10UF 20% 6.3V X5R 603
C2910 0.1uF 20% 10V CERM 402
C2911 0.1uF 20% 10V CERM 402
C2912 0.1uF 20% 10V CERM 402
C2913 0.1uF 20% 10V CERM 402
C2914 0.1uF 20% 10V CERM 402
C2915 0.1uF 20% 10V CERM 402
C2916 0.1uF 20% 10V CERM 402
C2917 0.1uF 20% 10V CERM 402
C2918 0.1uF 20% 10V CERM 402
C2919 0.1uF 20% 10V CERM 402
C2920 0.1uF 20% 10V CERM 402
C2921 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	07001
SCALE: NONE	SHT 29 OF 81	

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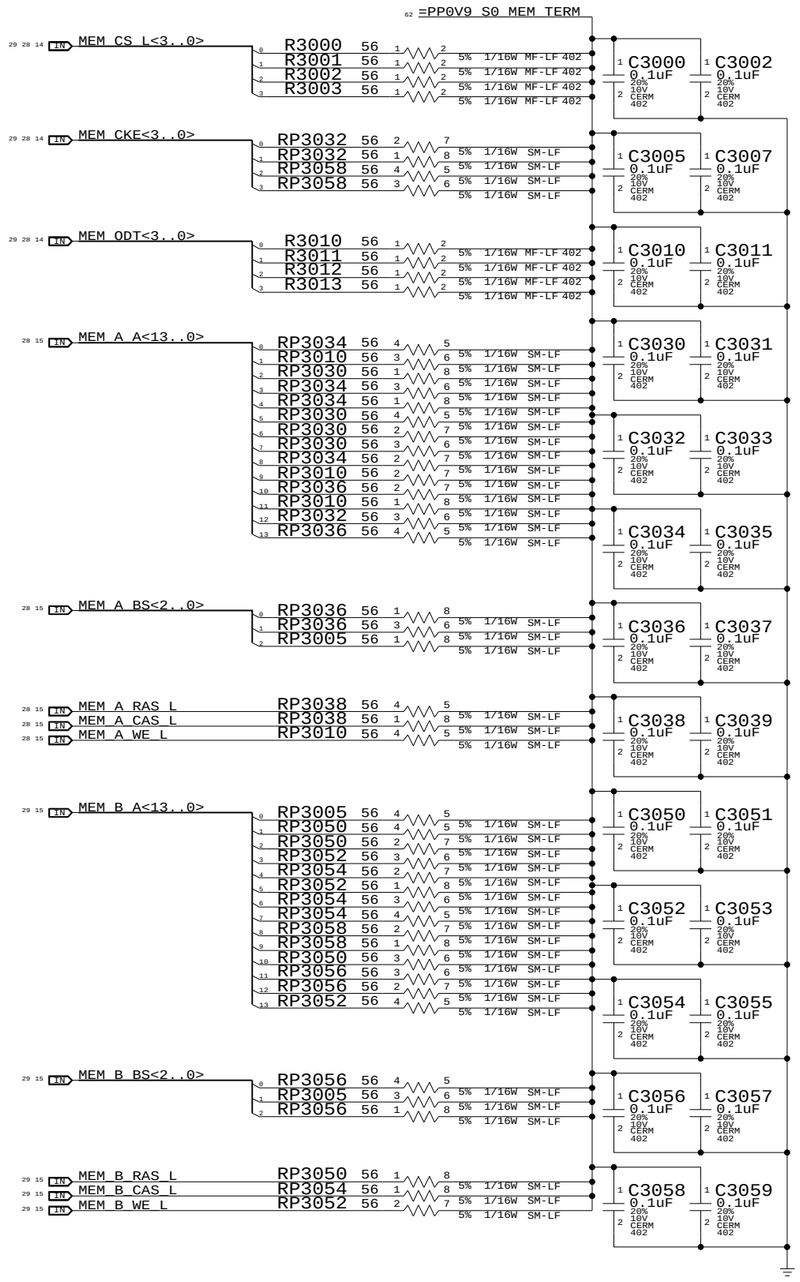
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	30	81

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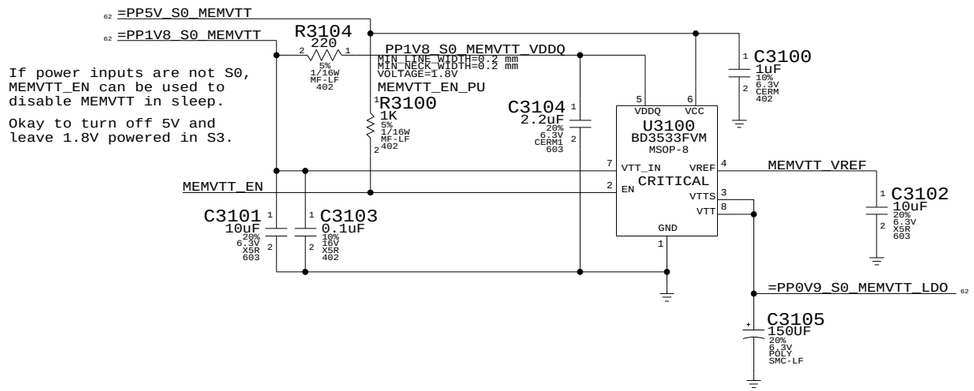
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	31	81

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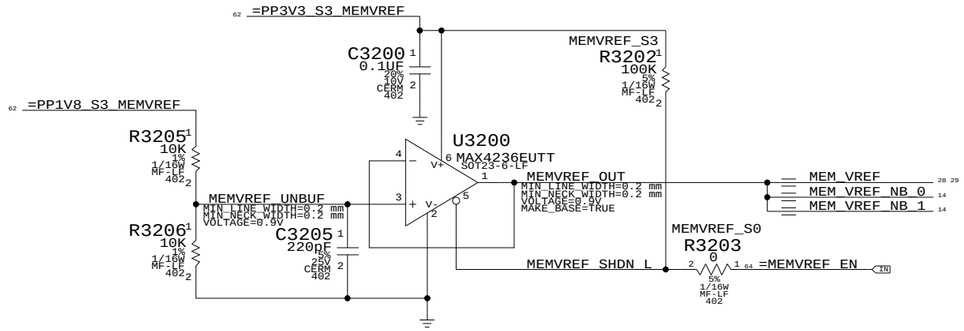

DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	32	81

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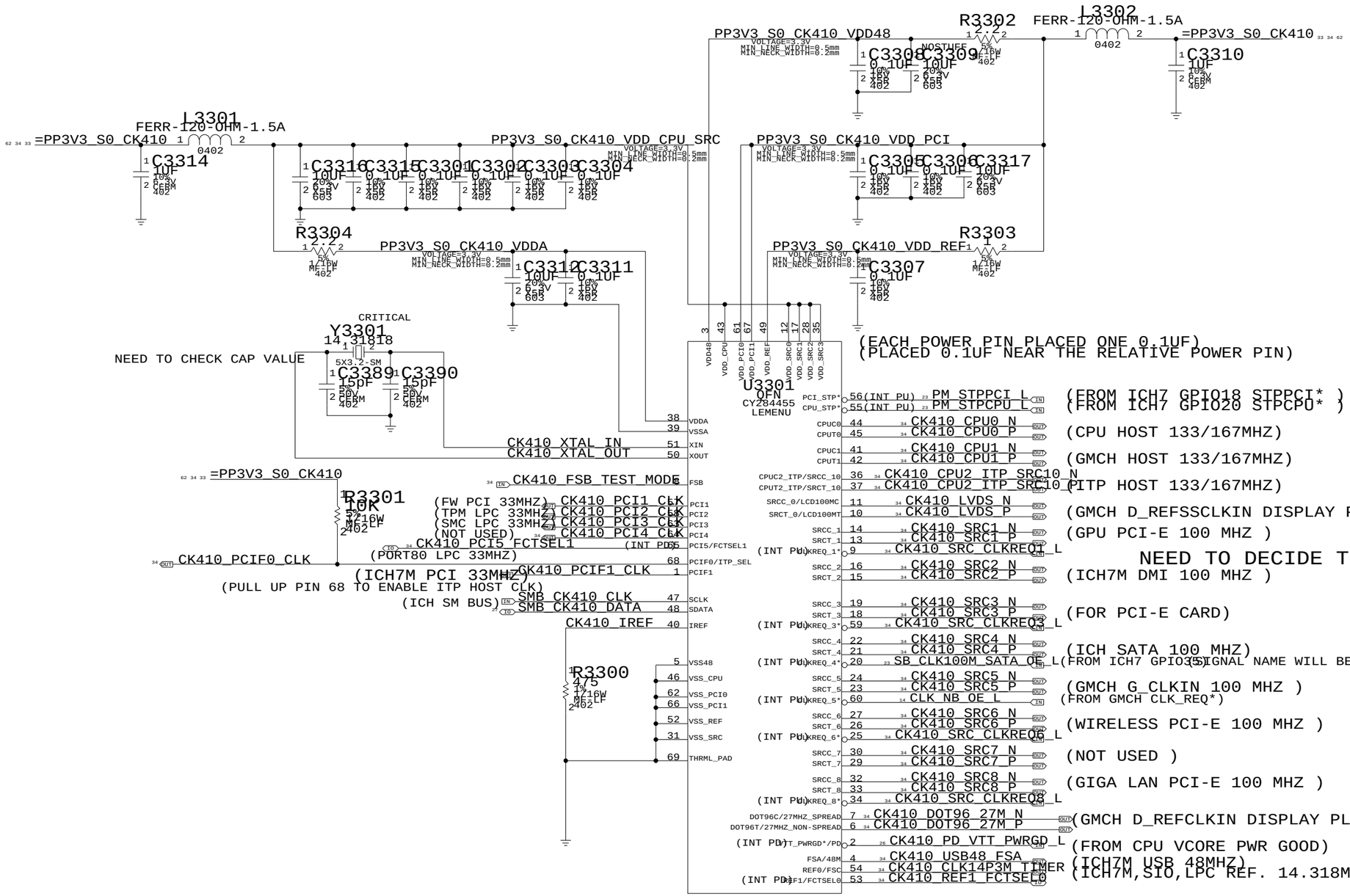

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF	LOW	BD	SRCT0	SRCC0

CLOCKS

SYNC_MASTER=MAC SYNC_DATE=09/08/2005

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SCALE	SHT	OF
NONE	33	81

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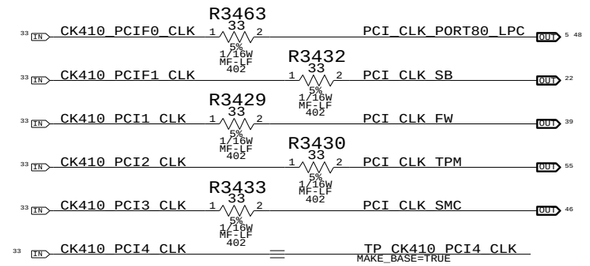
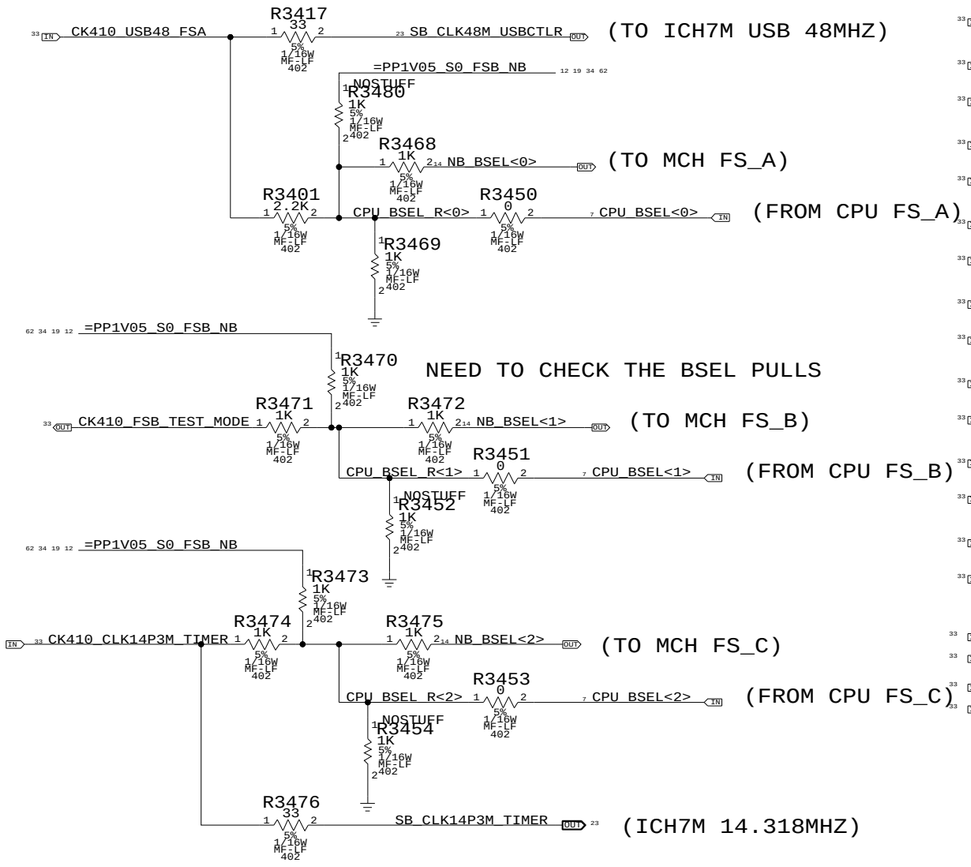
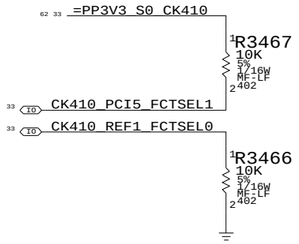


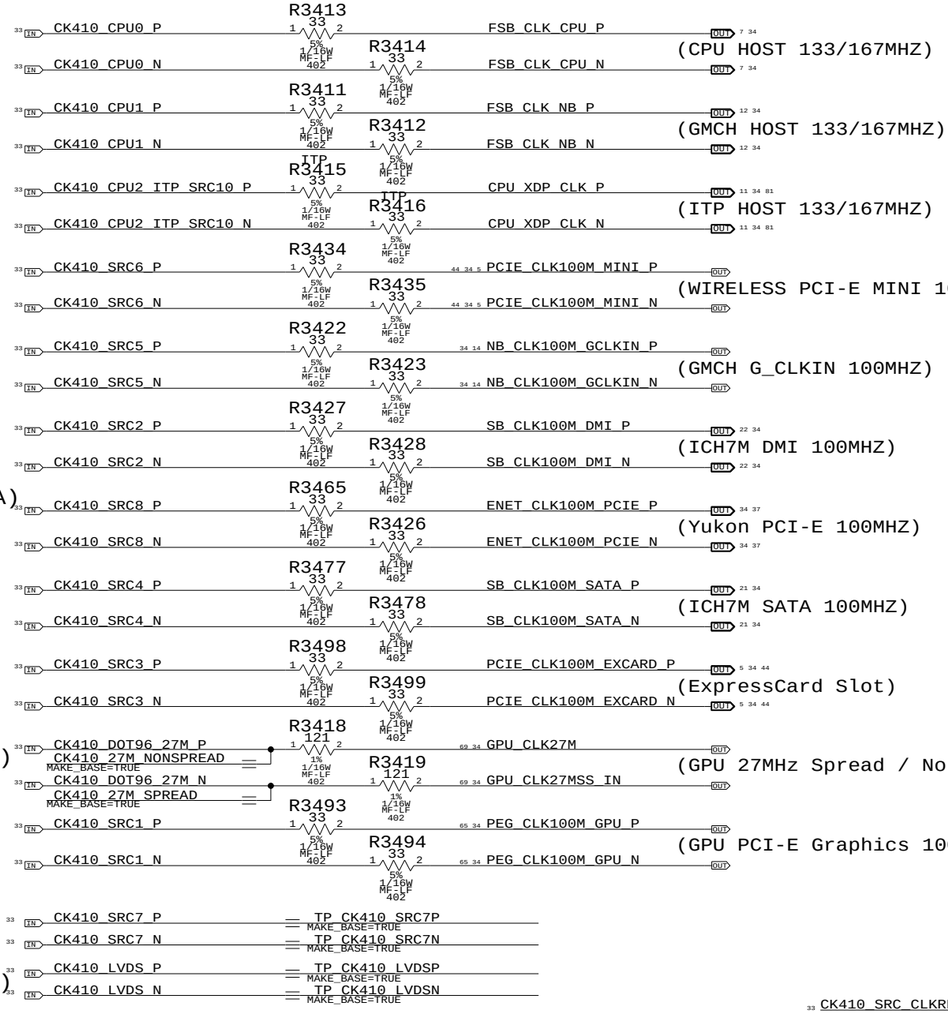


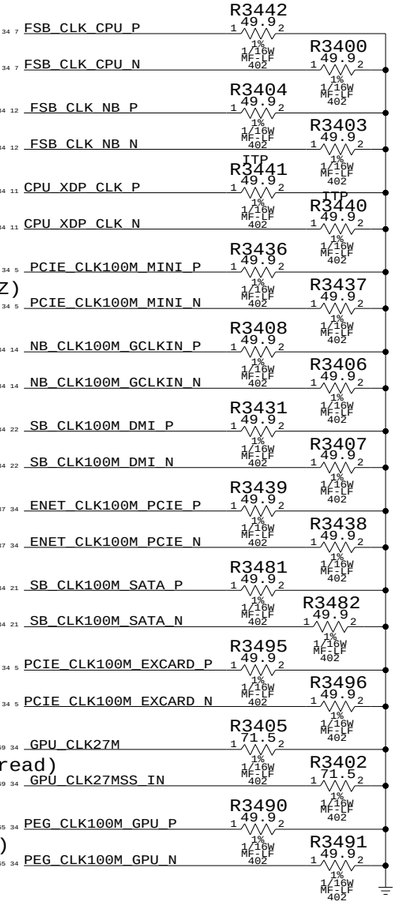


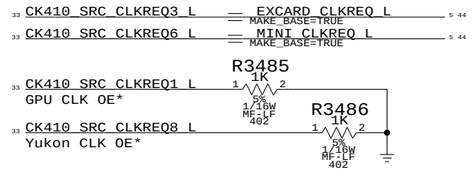
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
0	0	0	266M
# 0	0	1	133M
# 0	1	0	166M
0	1	1	200M
1	0	0	100M
1	0	1	333M
1	1	0	400M
1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED







Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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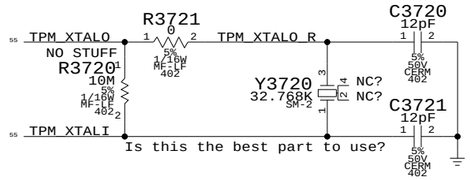
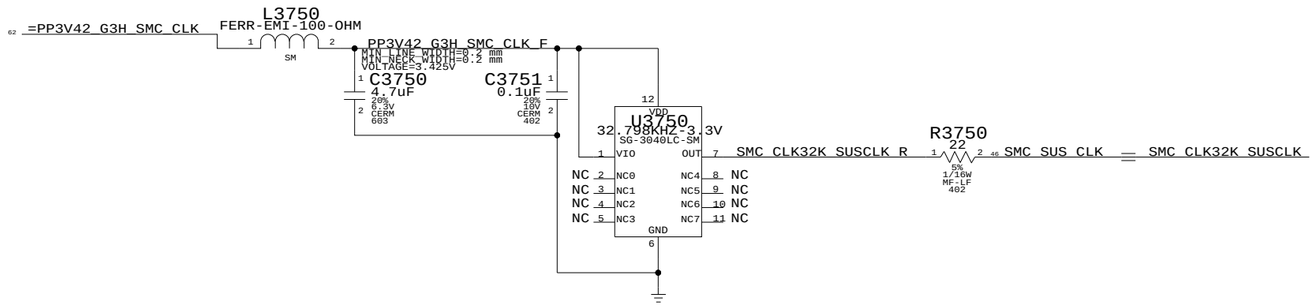
TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	35	81

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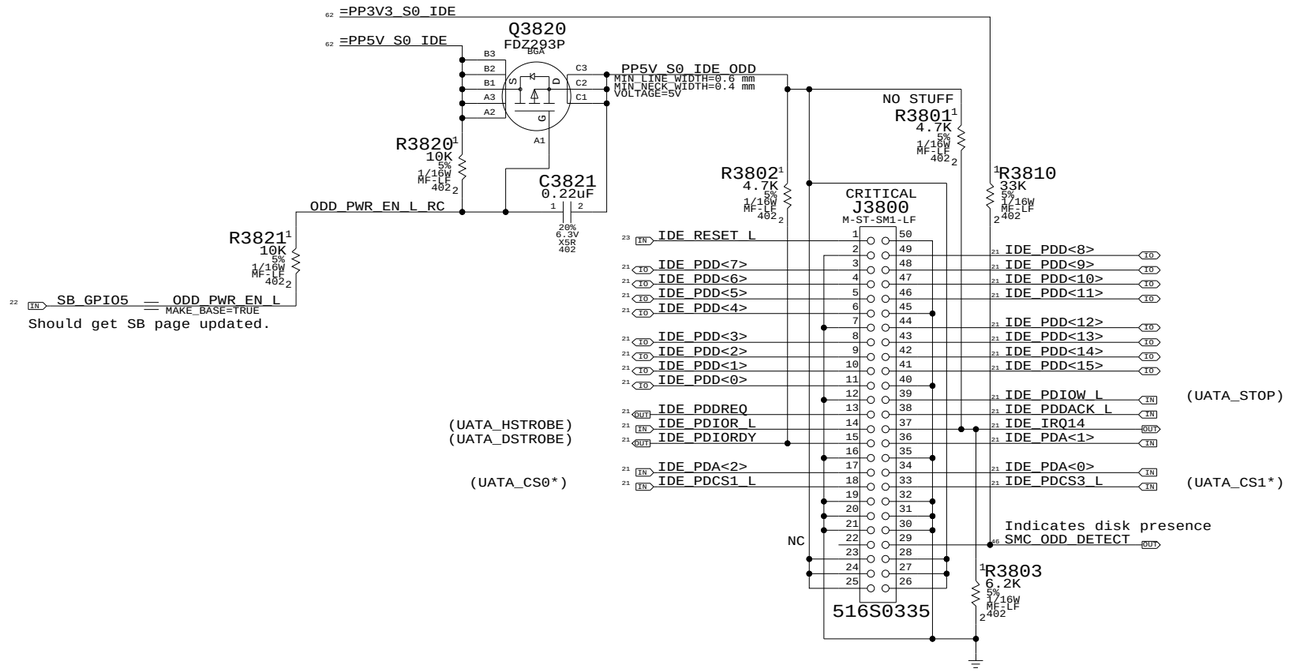
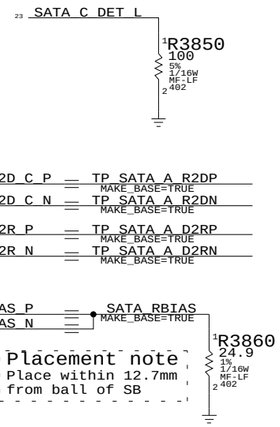
IDE (ODD) Connector





PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	36	81

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PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402 =PP2V5_S3_ENET

PLACE C4107 NEAR U4101 AVDD

=PP3V3_S3_ENET
=PP1V2_S3_ENET
=PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF 10% 16V X5R 402
C4113 0.1UF 10% 16V X5R 402

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N
ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_GATED_RST_L

LEMENU
U4101
88E8053
QFN

OPTIONAL EXTERNAL LDO

ANALOG
PCI EXPRESS
LED
MEDIA
TEST
TWSI
SPI
MAIN CLK

ENET_LOM_DIS_L
ENET_CTRL25
ENET_CTRL12
ENET_RSET
NO PULL-UP NEEDED
R4102 4.87K 1% 1/16W MF-LF 402

LOM_DISABLE*
VAUX_AVLBL
VMAIN_AVLBL
SWITCH_VCC
SWITCH_VAUX
HSDACP
HSDACN
CTRL25
CTRL12
RSET
LED_ACT*
LED_LINK10/100*
LED_LINK1000*
LINK*
TSTPT
TESTMODE

MDIP0 MDIN0 MDIP1 MDIN1 MDIP2 MDIN2 MDIP3 MDIN3
ENET_MDI_P<0> ENET_MDI_N<0> ENET_MDI_P<1> ENET_MDI_N<1> ENET_MDI_P<2> ENET_MDI_N<2> ENET_MDI_P<3> ENET_MDI_N<3>

R4106 R4105 R4104 R4103 R4120 R4119 R4118 R4117
49.9 1% 1/16W MF-LF 402

ENET_MDI0 ENET_MDI1 ENET_MDI2 ENET_MDI3

C4116 C4115 C4117 C4118
0.001UF 10% 50V CERM 402

VPD_CLK ENET_VPD_CLK
VPD_DATA ENET_VPD_DATA

PU_VDDO_TTL0 ENET_PU_VDD_TTL0
PU_VDDO_TTL1 ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 8053

SPI_DI NC
SPI_DO NC
SPI_CLK NC
SPI_CS NC

INTERNAL PULL-UP

CRITICAL
XTALI ENET_XTALI
XTALO ENET_XTALO
Y4101 25.0000M SM-3
C4150 22pF 5% 50V CERM 402
C4151 22pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

THRML_PAD

PLACE RESISTORS CLOSE TO U4101

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

LEMENU
U4102 M24C08 SO8
VCC VSS E2 NC1 NC0 WC* SDA SCL

ENET_VPD_DATA
ENET_VPD_CLK

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

C4126 C4127 C4128 C4129 C4130 C4131 C4132 C4133 C4134
0.1UF 10% 16V X5R 402
0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

C4135 C4136 C4137 C4138 C4139
0.1UF 10% 16V X5R 402
0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=09/08/2005

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NONE	37	81

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

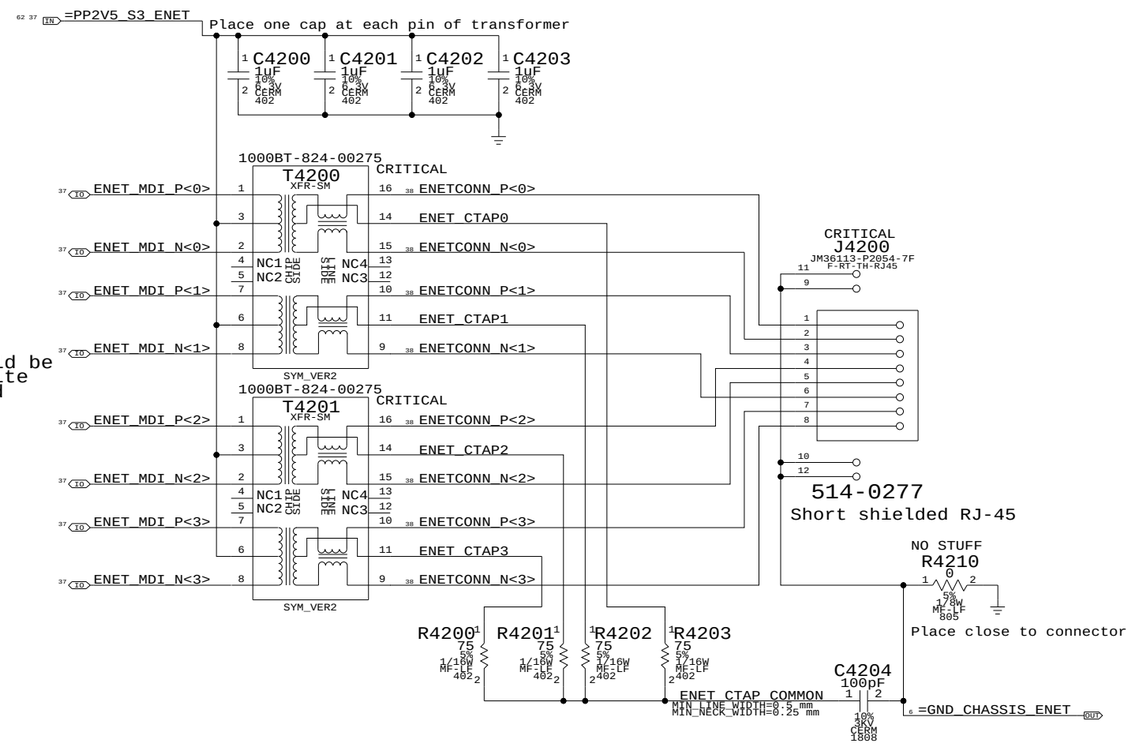
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	07001

SCALE	SHT	OF
NONE	38	81

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PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW23506 ADDED
6/21/2005 - CHANGED INT*_TO_INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_IO_TO_ADx (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT_TO_REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_FW_DIFF_PAIR_NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

62 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 10% 16V X5R 402
C4422 0.1UF 10% 16V CERM 402
C4426 0.1UF 10% 16V CERM 402
C4428 0.1UF 10% 16V CERM 402
C4430 0.1UF 10% 16V CERM 402
C4432 0.1UF 10% 16V CERM 402

L4400
600-OHM-300MA
0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 16V X5R 402
C4429 0.1UF 10% 16V X5R 402
C4425 0.1UF 10% 16V X5R 402

62 =PP3V3_S3_PCI

CONNECT TO VDD FOR 3.3V OPERATION

U4400
FW32306
BGA
LEMENU

197S0030 3.2MMX2.5MM CRITICAL
Y4403 SM-2 24.576MHZ
R4400 390 5% 1/16W MF-LF 402
C4411 15PF 5% 50V CERM 402
C4412 15PF 5% 50V CERM 402
NEED TO CHECK CRYSTAL LOAD CAPACITANCE

SPEC RECOMMENDS 2.49K
R4452 2.49K 1% 1/16W MF-LF 402
C4420 0.1UF 10% 16V X5R 402
R4420 510K 5% 1/16W MF-LF 402

R4431 22 5% 1/16W MF-LF 402

R4432 100 5% 1/16W MF-LF 402
THIS IS FROM ICH-7M

MODE FOR EXTERNAL LINK
DUAL PORT DEVICES ARE POWER CLASS 4 (‘100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (‘000’)
LOW = NOT BUS MANAGER
LOW = PCI OPERATION

MANUFACTURING TEST PINS

FIREWIRE CONTROLLER

SYNC_MASTER=MSX SYNC_DATE=08/29/2005

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SCALE: NONE | SHT 39 OF 81

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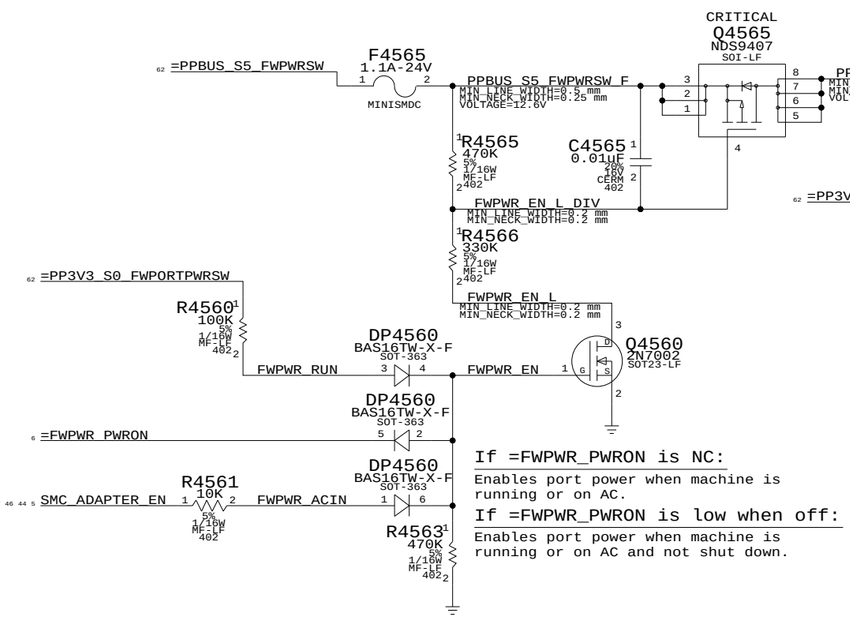
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch



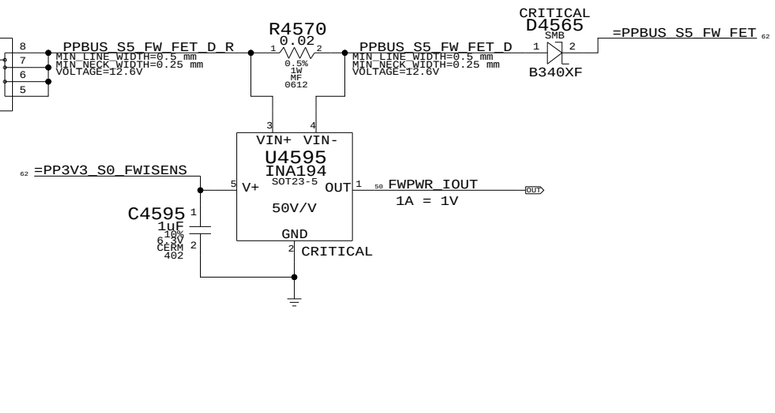
If =FWPWR_PWRON is NC:

Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:

Enables port power when machine is running or on AC and not shut down.

FireWire Port Current Sense



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	40	81

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY PHY PAGE	FW	FW_110D	FW_PORT1_TPA_FL_P 41
	FW	FW_110D	FW_PORT1_TPA_FL_N 41
	FW	FW_110D	FW_PORT1_TPB_FL_P 41
	FW	FW_110D	FW_PORT1_TPB_FL_N 41

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

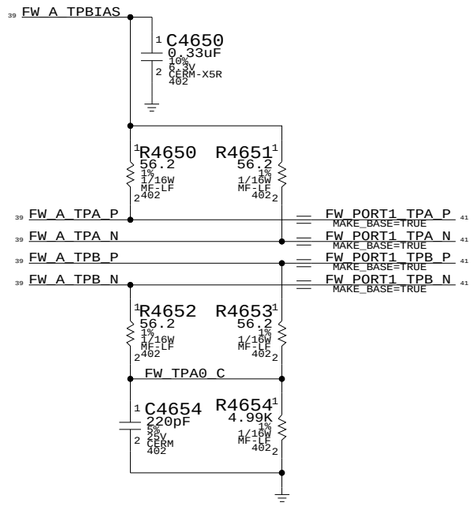
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

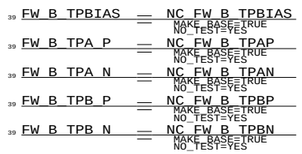
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

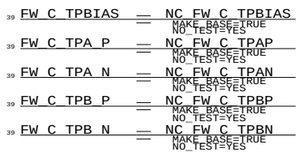
Place close to FireWire PHY



2nd TPA/TPB pair unused

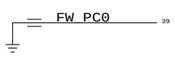

39 FW_B_TPBIAS — NC_FW_B_TPBIAS MAKE_BASE=TRUE NO_TEST=YES
39 FW_B_TPA_P — NC_FW_B_TPAP MAKE_BASE=TRUE NO_TEST=YES
39 FW_B_TPA_N — NC_FW_B_TPAN MAKE_BASE=TRUE NO_TEST=YES
39 FW_B_TPB_P — NC_FW_B_TPBP MAKE_BASE=TRUE NO_TEST=YES
39 FW_B_TPB_N — NC_FW_B_TPBN MAKE_BASE=TRUE NO_TEST=YES

3rd TPA/TPB pair unused

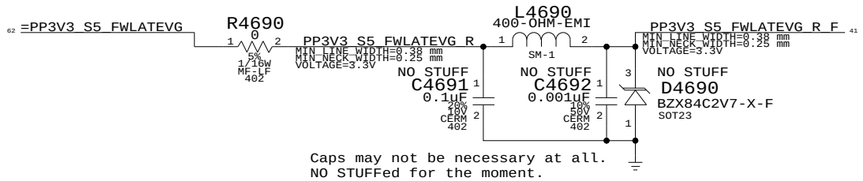

39 FW_C_TPBIAS — NC_FW_C_TPBIAS MAKE_BASE=TRUE NO_TEST=YES
39 FW_C_TPA_P — NC_FW_C_TPAP MAKE_BASE=TRUE NO_TEST=YES
39 FW_C_TPA_N — NC_FW_C_TPAN MAKE_BASE=TRUE NO_TEST=YES
39 FW_C_TPB_P — NC_FW_C_TPBP MAKE_BASE=TRUE NO_TEST=YES
39 FW_C_TPB_N — NC_FW_C_TPBN MAKE_BASE=TRUE NO_TEST=YES

FW Power Class Strap

Single-port system sets PC=0

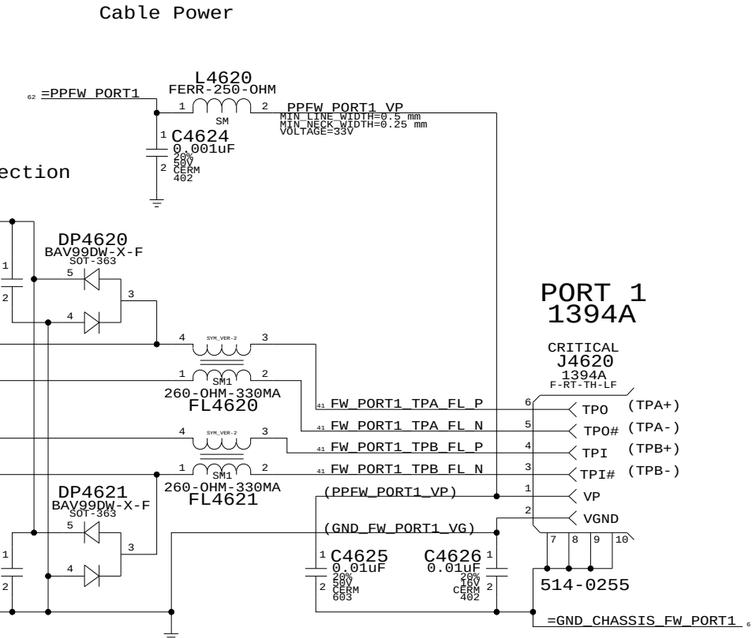


Late-VG Protection Power

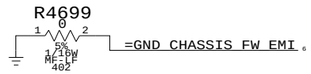


Caps may not be necessary at all.
NO STUFFed for the moment.

Cable Power



"Snapback" & "Late VG" Protection



FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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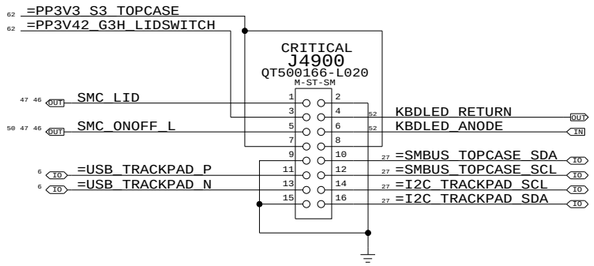
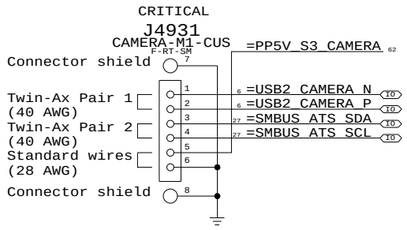
Top-Case Connector



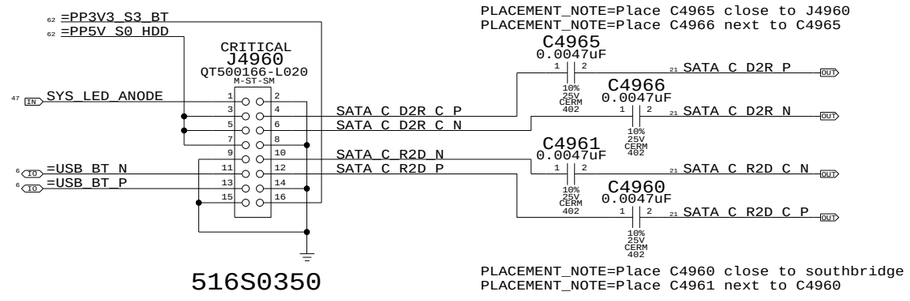
516S0350

Camera Connector



518S0371

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

Internal USB Connections

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	NONE	42	81

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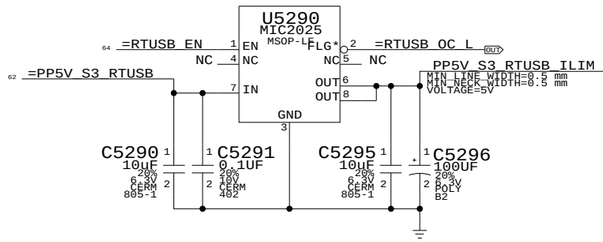
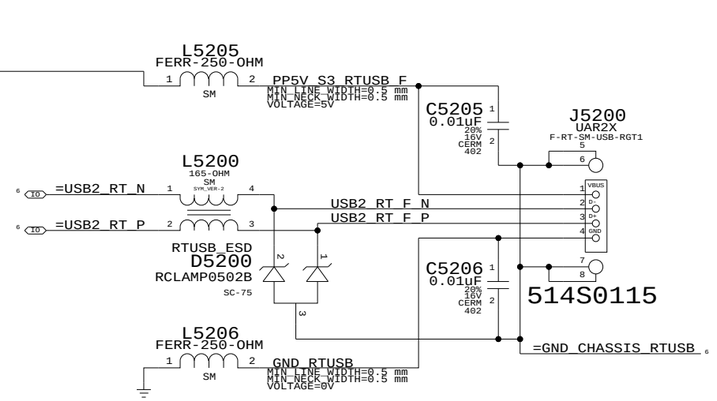
Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	43	81

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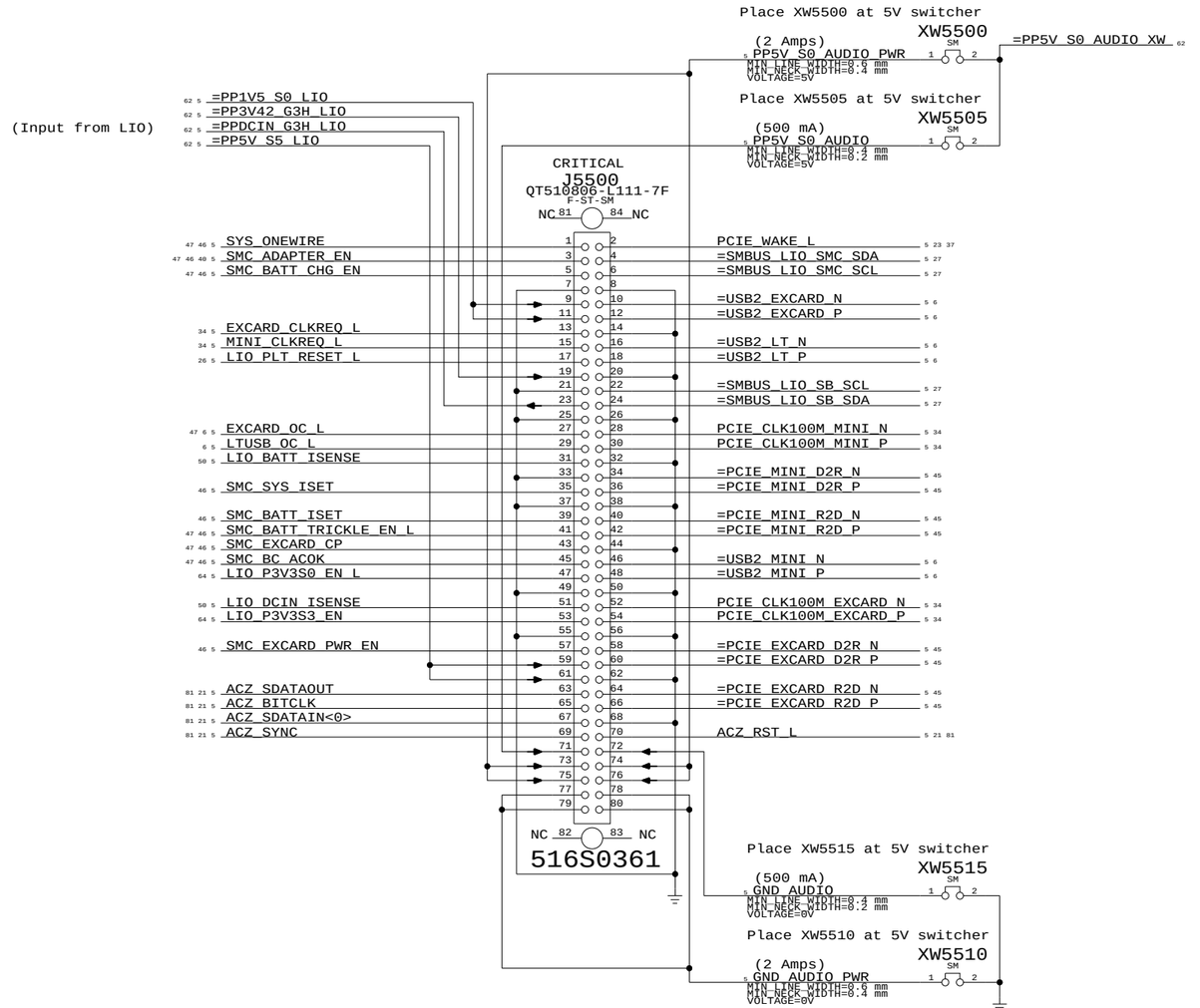
Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NONE	44	81

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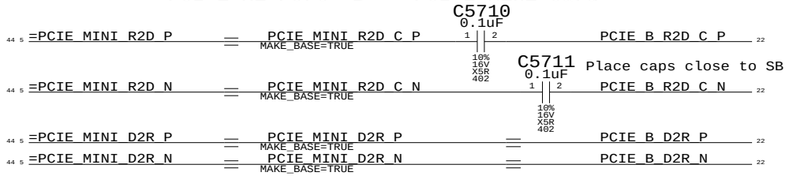
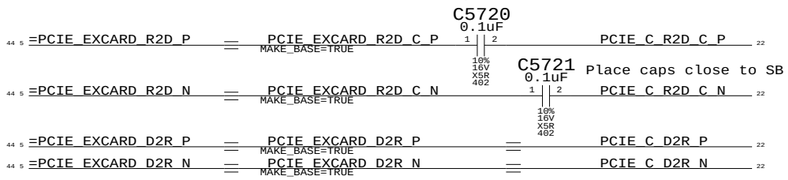
PCI-E x1 Port "A" = Ethernet (Yukon)

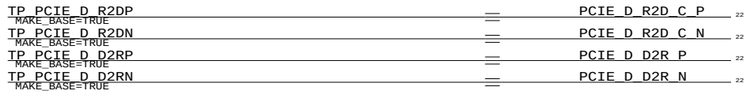
PCI-E x1 Port "B" = PCI-E Mini Card



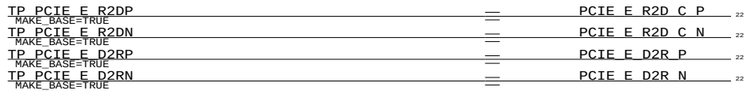
PCI-E x1 Port "C" = ExpressCard



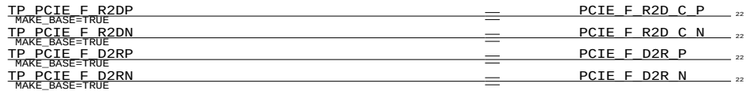
PCI-E x1 Port "D" = Unused



PCI-E x1 Port "E" = Unused



PCI-E x1 Port "F" = Unused



PCI-E Connections

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UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SETS BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

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U5800
SMC_H8S2116
BGA
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PM_LAN_ENABLE	B12	P10	
SMC_RSTGATE_L	C13	P11	
ALL_SYS_PWRGD	A15	P12	
RSMRST_PWRGD	B14	P13	
SMC_SB_NMI	B15	P14	
PM_RSMRST_L	C14	P15	
IMVP_VR_ON	D12	P16	
PM_PWRBTN_L	C15	P17	
SMC_P20	D13	P20	
SMC_P21	D14	P21	
SMC_P22	D15	P22	
SMC_P23	E12	P23	
SMC_BATT_TRICKLE_EN	E14	P24	
SMC_BATT_CHG_EN	E15	P25	
SMC_P26	E13	P26	
SMC_P27	F14	P27	
LPC_AD<0>	D9	P30/LAD0	
LPC_AD<1>	C9	P31/LAD1	
LPC_AD<2>	A9	P32/LAD2	
LPC_AD<3>	B9	P33/LAD3	
LPC_FRAME_L	D8	P34/LFRAME*	
SMC_LRESET_L	C8	P35/LRESET*	
PCI_CLK_SMC	A8	P36/LCLK	
INT_SERIRQ	D7	P37/SERIRQ	
SMC_XDP_TMS_L	A5	P40/TMI0	
SMC_XDP_TDI_L	B5	P41/TMO0	
SMB_BSB_DATA	D5	P42/SDA1	
SMC_TPM_PP	C3	P43/TMI1/EXSCKL	
SMC_XDP_TRST_L	B1	P44/TMO1	
SMC_XDP_TCK	C2	P45	
SMC_SYS_LED	D3	P46/PWX0/PWM0	
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1	
SMC_TX_L	G1	P50	
SMC_RX_L	G4	P51	
SMC_SMB_0_CLK	F2	P52/SCL0	

P60/KIN0*	L13	64	SMC_PM_G2_EN
P61/KIN1*	L14	47 44 40 5	SMC_ADAPTER_EN
P62/KIN2*	L15	76 22	SPI_ARB
P63/KIN3*	K12	51 22	SPI_SCLK
P64/KIN4*	K13	76 51 22	SPI_SI
P65/KIN5*	K14	76 51 22	SPI_SO
P66/IRQ6*/KIN6*	J12	47	SMC_PROCHOT_3_3_L
P67/IRQ7*/KIN7*	J13	47	SMC_CPU_INIT_3_3_L
P70/AN0	N12	50	SMC_CPU_ISENSE
P71/AN1	R13	50	SMC_CPU_VSENSE
P72/AN2	P13	50	SMC_GPU_ISENSE
P73/AN3	R14	50	SMC_GPU_VSENSE
P74/AN4	P14	50	SMC_DCIN_ISENSE
P75/AN5	R15	50	SMC_PBUS_VSENSE
P76/AN6	N13	50	SMC_BATT_ISENSE
P77/AN7	P15	50	SMC_FWIRE_ISENSE
P80/PME*	C7	23	SMC_WAKE_SCI_L
P81/GA20	A7	47	SMC_TPM_GPIO
P82/CLKRUN*	B7	55 48 39 23 5	PM_CLKRUN_L
P83/LPCPD*	D6	55 48 23 5	PM_SUS_STAT_L
P84/IRQ3*/TXD1	C6	47	SC_TX_L
P85/IRQ4*/RXD1	A6	47	SC_RX_L
P86/IRQ5*/SCK1/SCL1	B6	27	SMB_BSB_CLK
P90/IRQ2*	K4	50 47 42	SMC_ONOFF_L
P91/IRQ1*	J2	47 44 5	SMC_BC_ACOK
P92/IRQ0*	J1	63 47 5	SMC_BS_ALRT_L
P93/IRQ12*	J3	64 23	PM_SLP_S3_L
P94/IRQ13*	J4	64 23	PM_SLP_S4_L
P95/IRQ14*	H2	23	PM_SLP_S5_L
P96/EXCL	H1	35	SMC_SUS_CLK
P97/IRQ15*/SDA0	G2	27	SMC_SMB_0_DATA

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2PC	
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	
PM_EXTTS_L<0>	R1	PA4/KIN12*/PS2BC	
PM_THRM_L	N2	PA5/KIN13*/PS2BD	
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	
SMC_EXTSMI_L	B10	PB0/LSMI*	
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	
SMC_ODD_DETECT	D10	PB2	
ISENSE_CAL_EN	A11	PB3	
SMC_EXCARD_CP	B11	PB4	
SMC_EXCARD_PWR_EN	C11	PB5	
SMC_EXCARD_PWR_OC_L	A12	PB6	
SMC_XDP_TDO_3_3_L	D11	PB7	
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	
SMS_X_AXIS	M11	PD0/AN8	
SMS_Y_AXIS	P11	PD1/AN9	
SMS_Z_AXIS	R11	PD2/AN10	
SMC_ANALOG_ID	N11	PD3/AN11	
SMC_NB_ISENSE	P10	PD4/AN12	
SMC_MEM_ISENSE	R10	PD5/AN13	
ALS_LEFT	N10	PD6/AN14	
ALS_RIGHT	M10	PD7/AN15	

PE0	M3	47	SMC_CASE_OPEN
PE1*/ETCK	M2	48 47 5	SMC_TCK
PE2*/ETDI	M1	48 47 5	SMC_TDI
PE3*/ETDO	L4	48 47 5	SMC_TDO
PE4*/ETMS	L2	48 47 5	SMC_TMS
PF0/IRQ8*/PWM2	M7		SMC_PF0 47
PF1/IRQ9*/PWM3	P6		SMC_PF1 47
PF2/IRQ10*/TMOY	R6	47 42	SMC_LID
PF3/IRQ11*/TMOX	N6	47	SMC_CPU_RESET_3_3_L
PF4/PWM4	M6	44 5	SMC_BATT_ISET
PF5/PWM5	R5	47	SMC_BATT_VSET
PF6/PWM6	P5	44 5	SMC_SYS_ISET
PF7/PWM7	N5	47	SMC_SYS_VSET
PG0/EXIRQ8*/TMIX	P9	76 51 22	SPI_CE_L
PG1/EXIRQ9*/TMIY	R9	76	SMC_XDP_TCK_3_3
PG2/EXIRQ10*/SDA2	N9	27	SMB_BSA_DATA
PG3/EXIRQ11*/SCL2	P8	27	SMB_BSA_CLK
PG4/EXIRQ12*/EXSDAA	R8	27	SMB_A_S3_DATA
PG5/EXIRQ13*/EXSCLA	M8	27	SMB_A_S3_CLK
PG6/EXIRQ14*/EXSDAB	P7	27	SMB_B_S0_DATA
PG7/EXIRQ15*/EXSCLB	R7	27	SMB_B_S0_CLK
PH0/EXIRQ6*	E1	47	SMC_PROCHOT
PH1/EXIRQ7*	F3	47	SMC_THRMTRIP
PH2/FWE	K2	47	SMC_FWE
PH3/EXEXCL	C4	52	ALS_GAIN
PH4	D4	47 23	SMS_INT_L
PH5	B3	54	SMS_ONOFF_L

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

62 47 46 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V X5R 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 20% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

VCL IS INTERNAL RAIL

62 47 46 =PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402
52 50 47 46 GND_SMC_AVSS

PP3V3_AVREF_SMC 47
62 47 46 =PP3V3_S5_SMC
R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402

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U5800
SMC_H8S2116
BGA
(3 OF 4)

48 47 5 SMC_RST_L
47 SMC_XTAL
47 SMC_EXTAL
KBC_MDE
SMC_MD1 5 48
SMC_NMI
SMC_TRST_L
R5898 10K 5% 1/16W MF-LF 402
R5803 10K 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402
NOSTUFF

XW5800
SM
GND_SMC_AVSS 46 47 50 52

SMC

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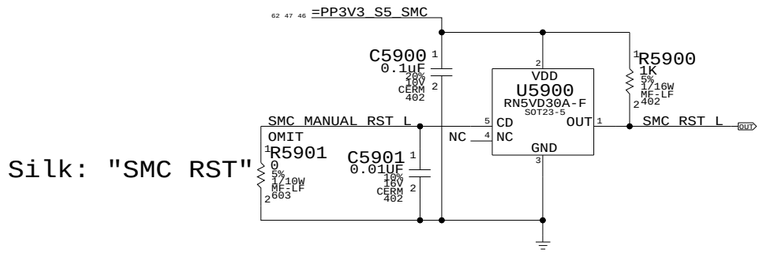
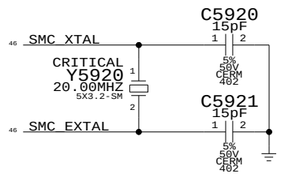
SMC Reset Button / Brownout Detect

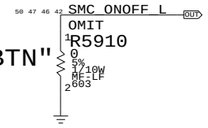


Silk: "SMC RST"

SMC Crystal Circuit

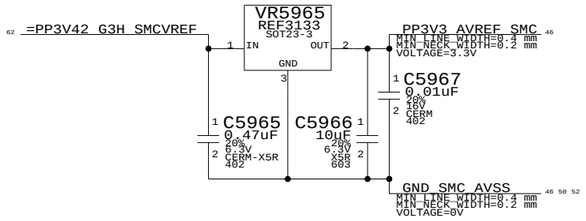


Debug Power Button

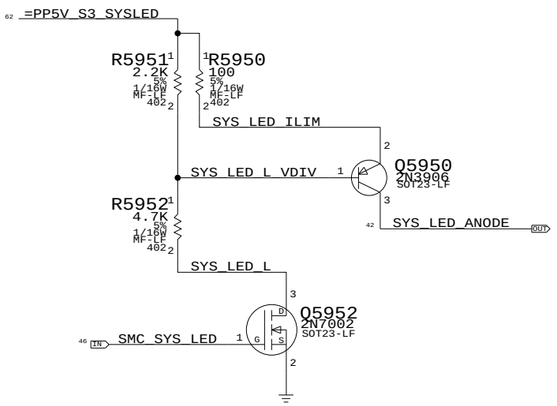


Silk: "PWR BTN"

SMC AVREF Supply

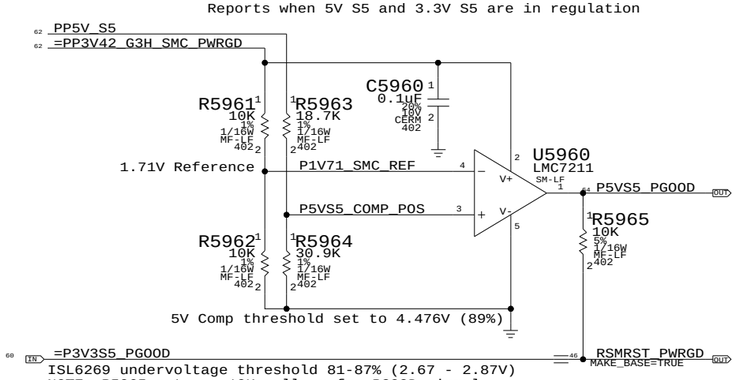


System (Sleep) LED Circuit

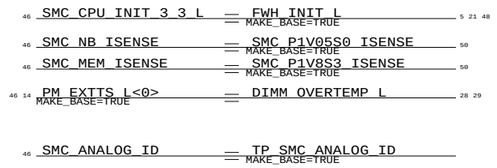


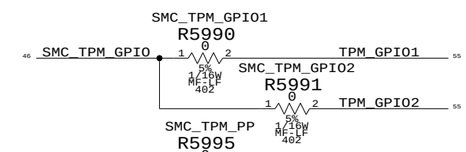
SMC PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation

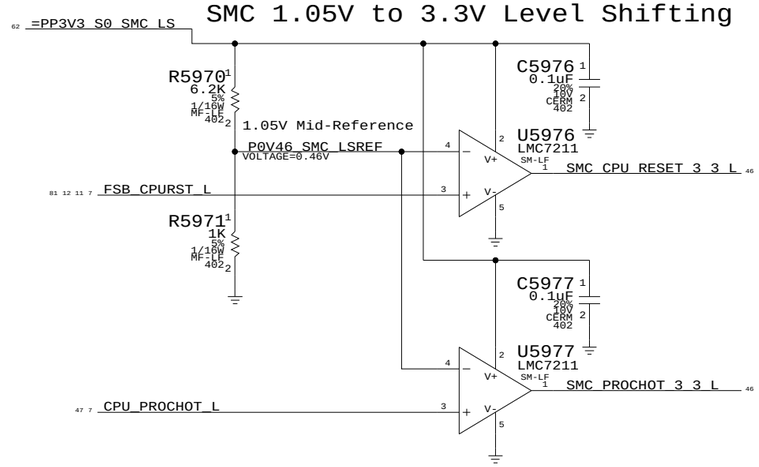


ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal

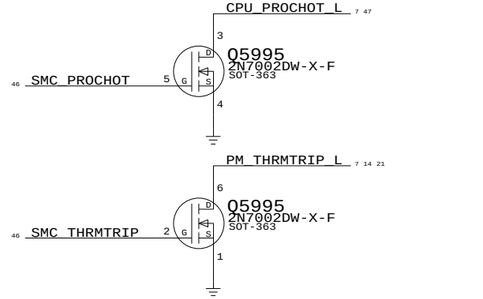


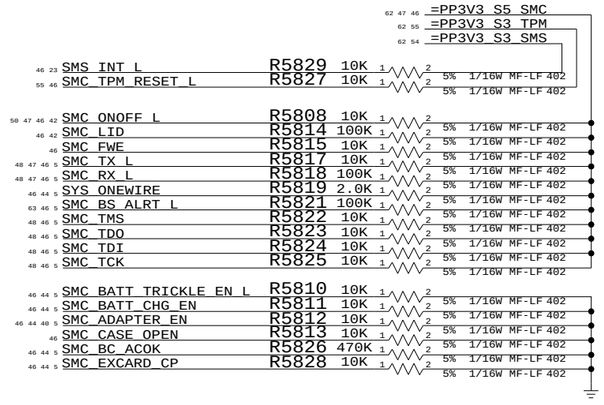


SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting





SMC Support

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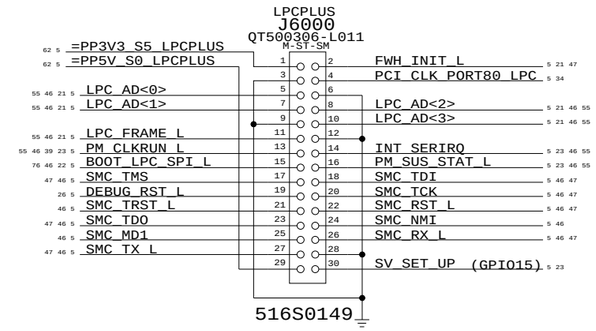

LPC+ Debug Connector

SYNC_MASTER=M42 SYNC_DATE=07/20/2005

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SCALE	SHT	OF
NONE	48	81

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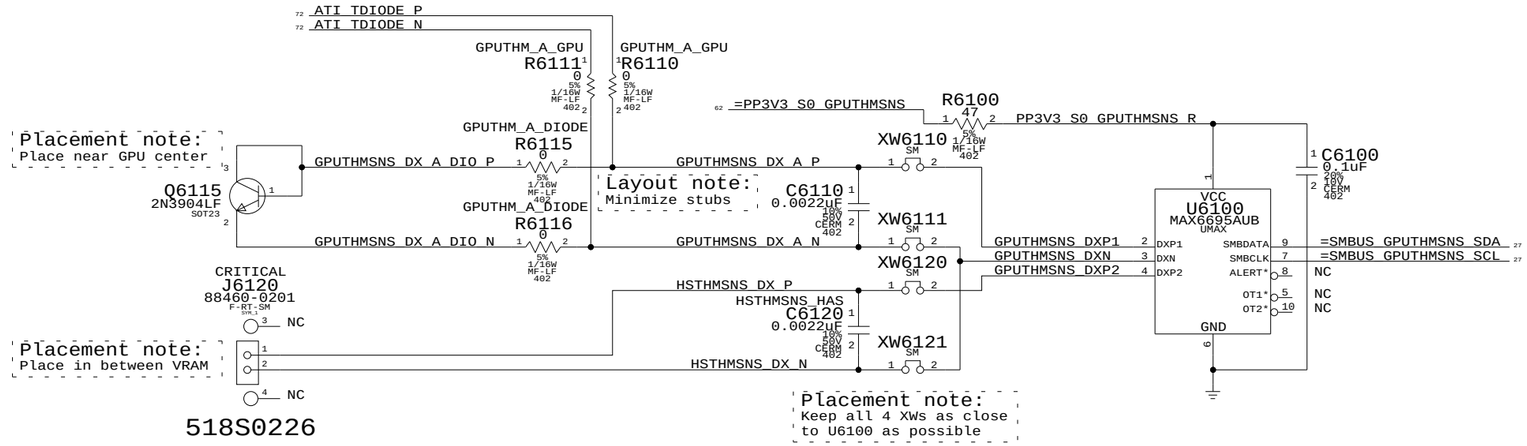
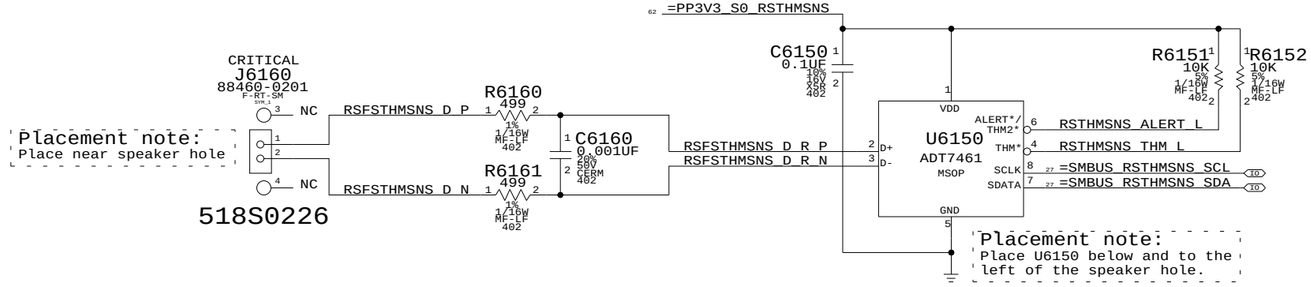
GPU / Heat Pipe Thermal Sensor

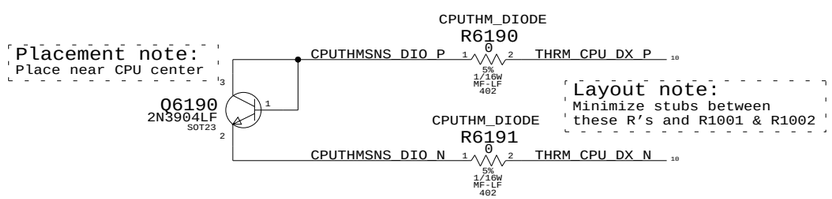


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

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D	051-6941	07001

SCALE	SHT	OF
NONE	49	81

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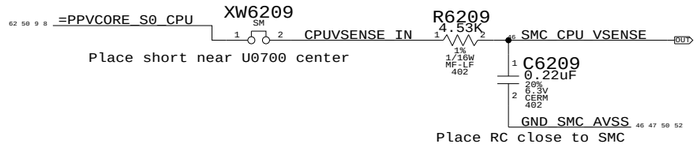
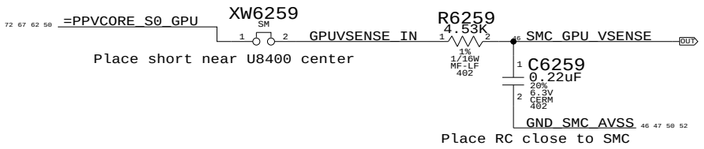
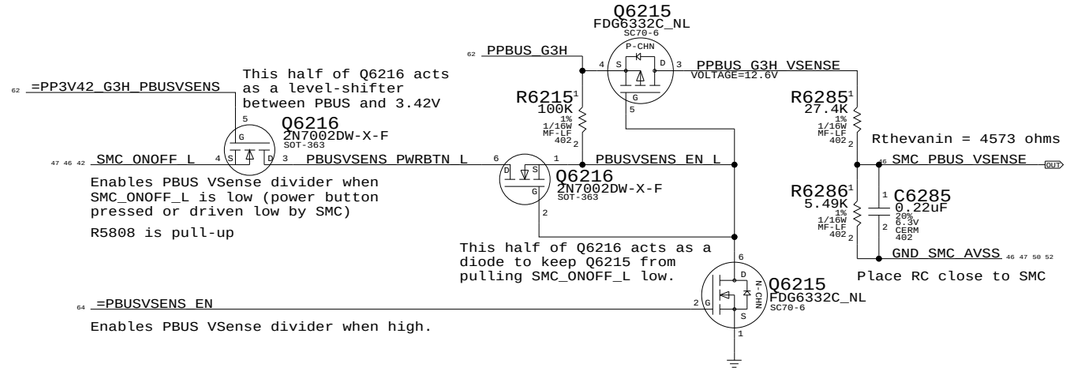
CPU Voltage Sense / Filter



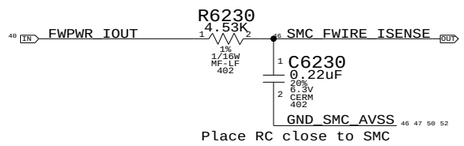
GPU Voltage Sense / Filter



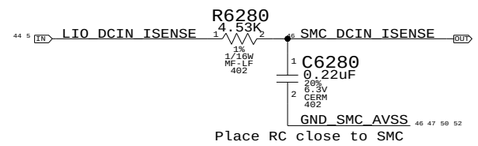
PBUS Voltage Sense Enable & Filter



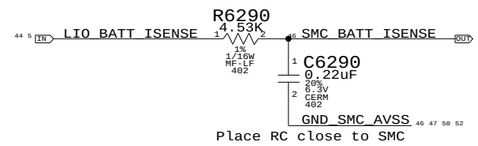
FireWire Current Sense Filter



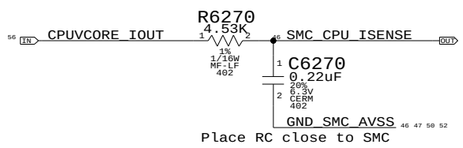
DCIN Current Sense Filter



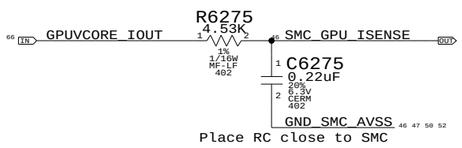
Battery Current Sense Filter



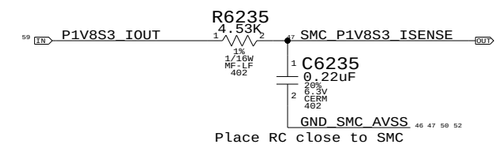
CPU Current Sense Filter



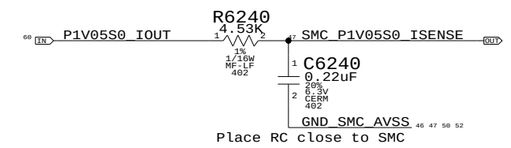
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

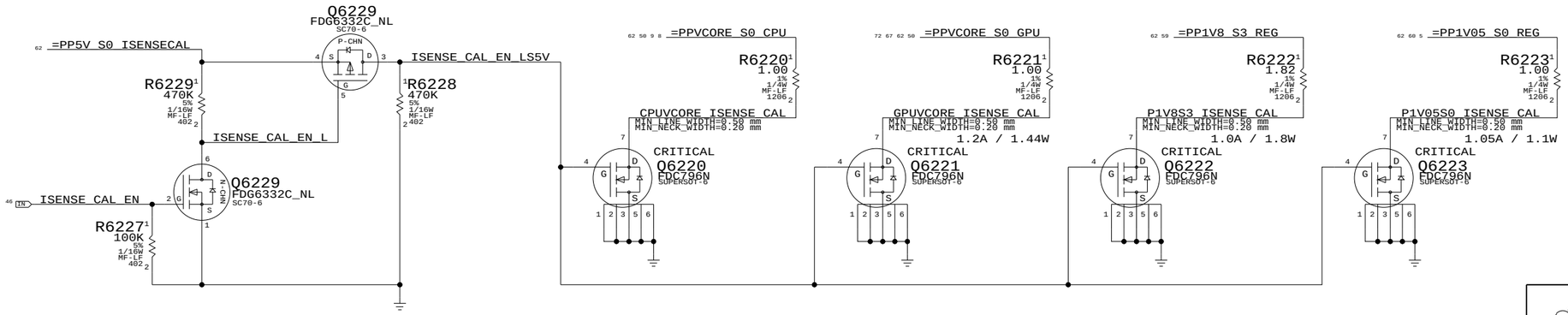


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing			
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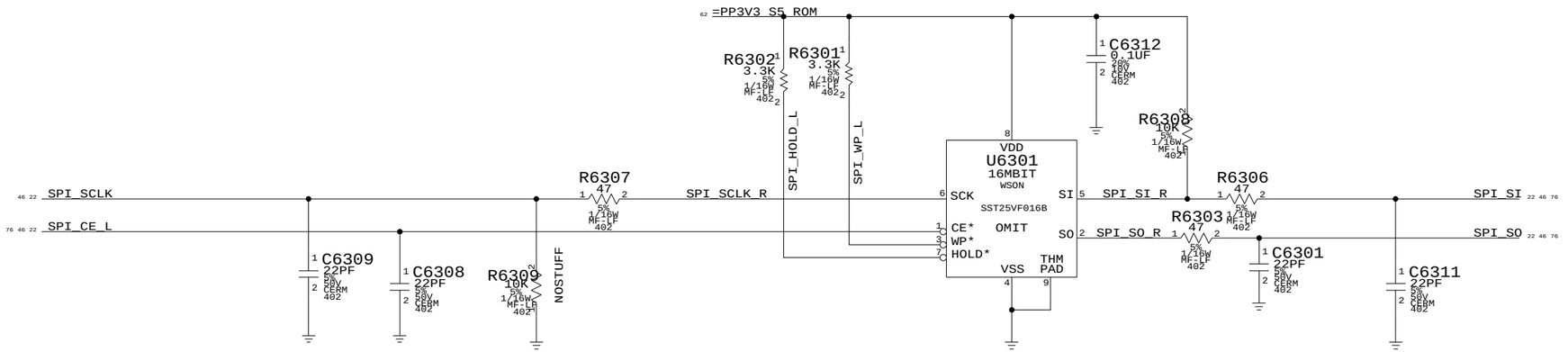

R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=(M42) SYNC_DATE=07/26/2005

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NONE	51	81

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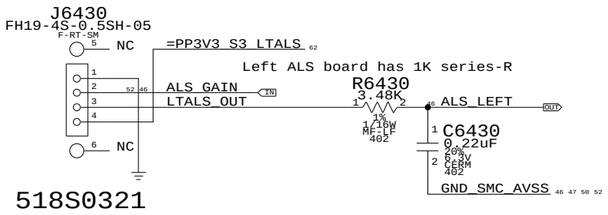
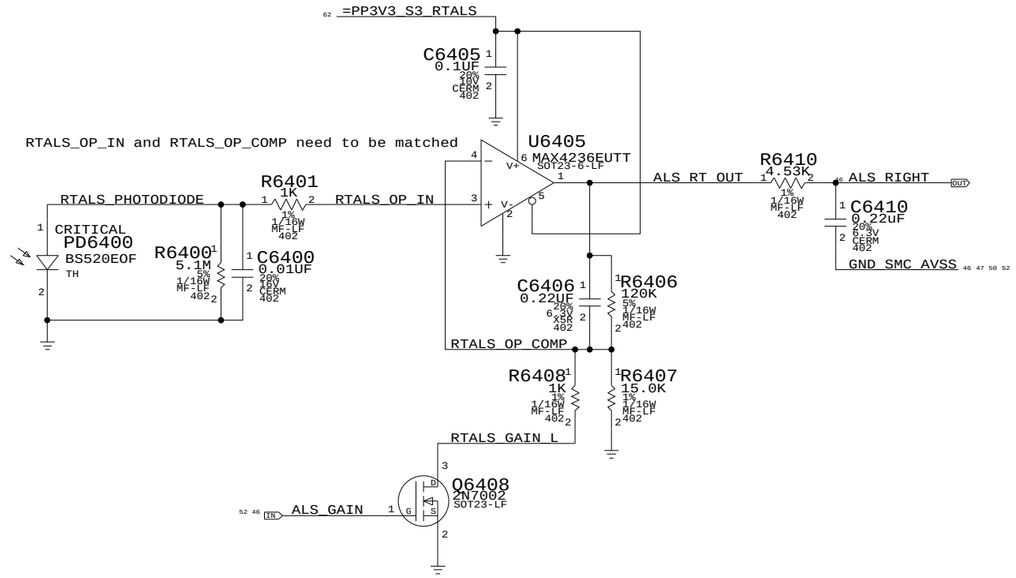
Left ALS "Connector"

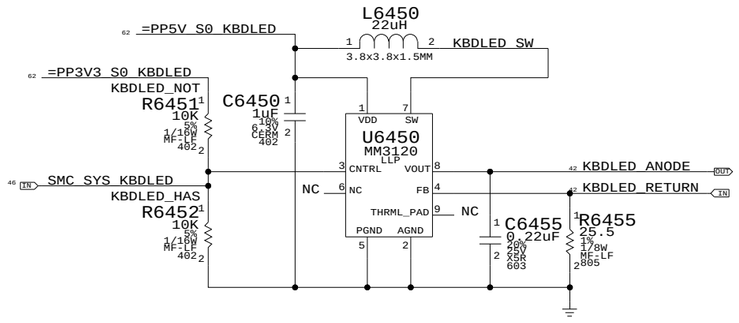


518S0321

Right ALS Circuit



Keyboard LED Driver



ALS Support

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NONE	52	81

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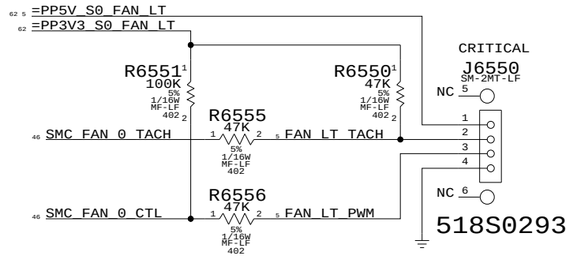
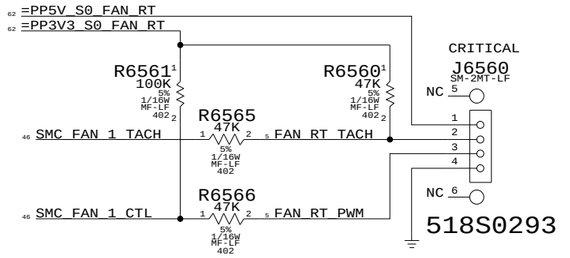
Left Fan



Right Fan



Fan Connectors

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SCALE	SHT	OF
NONE	53	81

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PAGE NOTES

INPUT

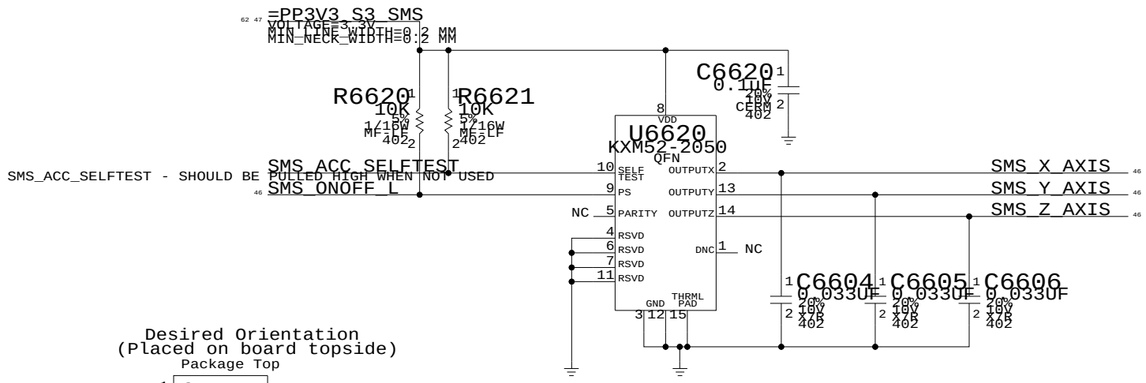
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT

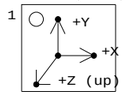
SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -



Desired Orientation
(Placed on board topside)
Package Top



SMS

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NONE	54	81

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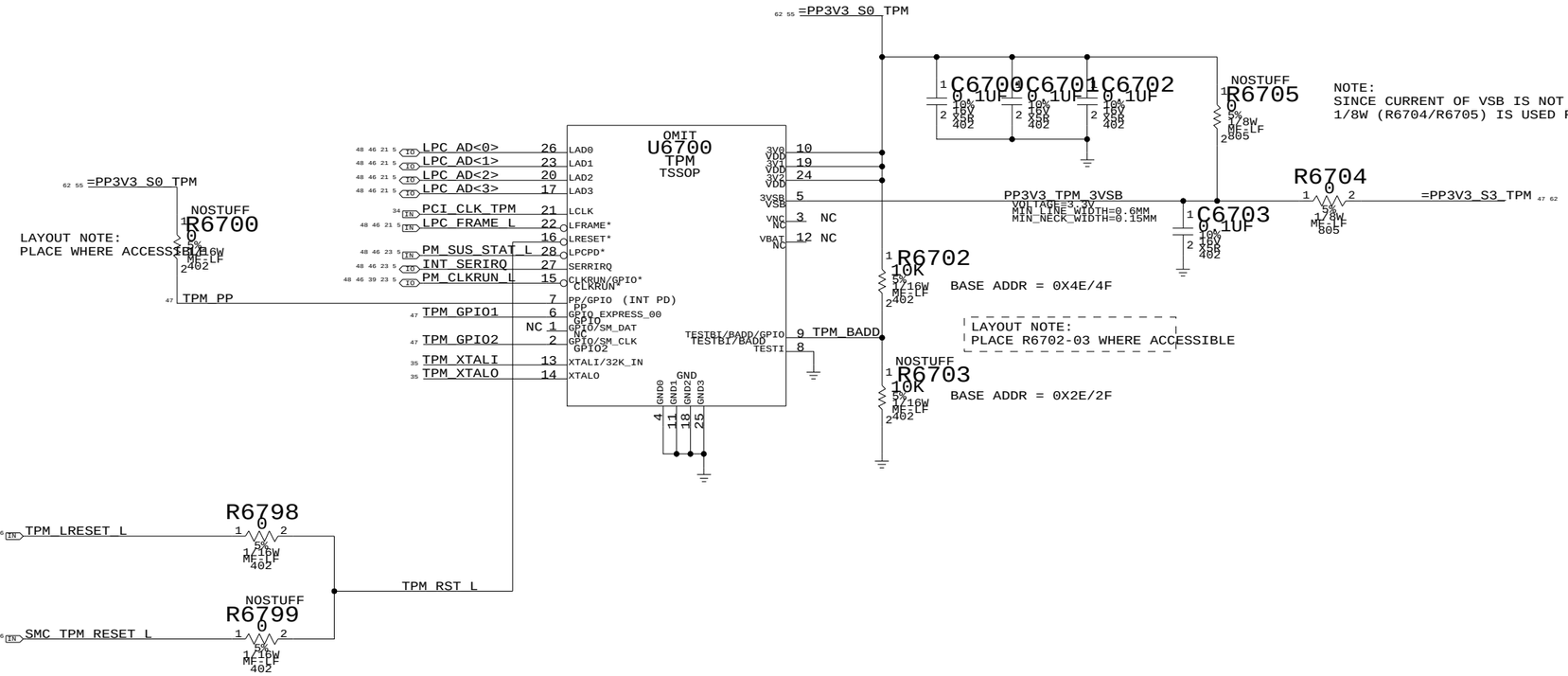

TPM

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D	051-6941	07001

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NONE	55	81

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DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

Vout = Variable
36A max output
(Inductors limit)

CPU VCore Current Sense

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 56 OF 81	

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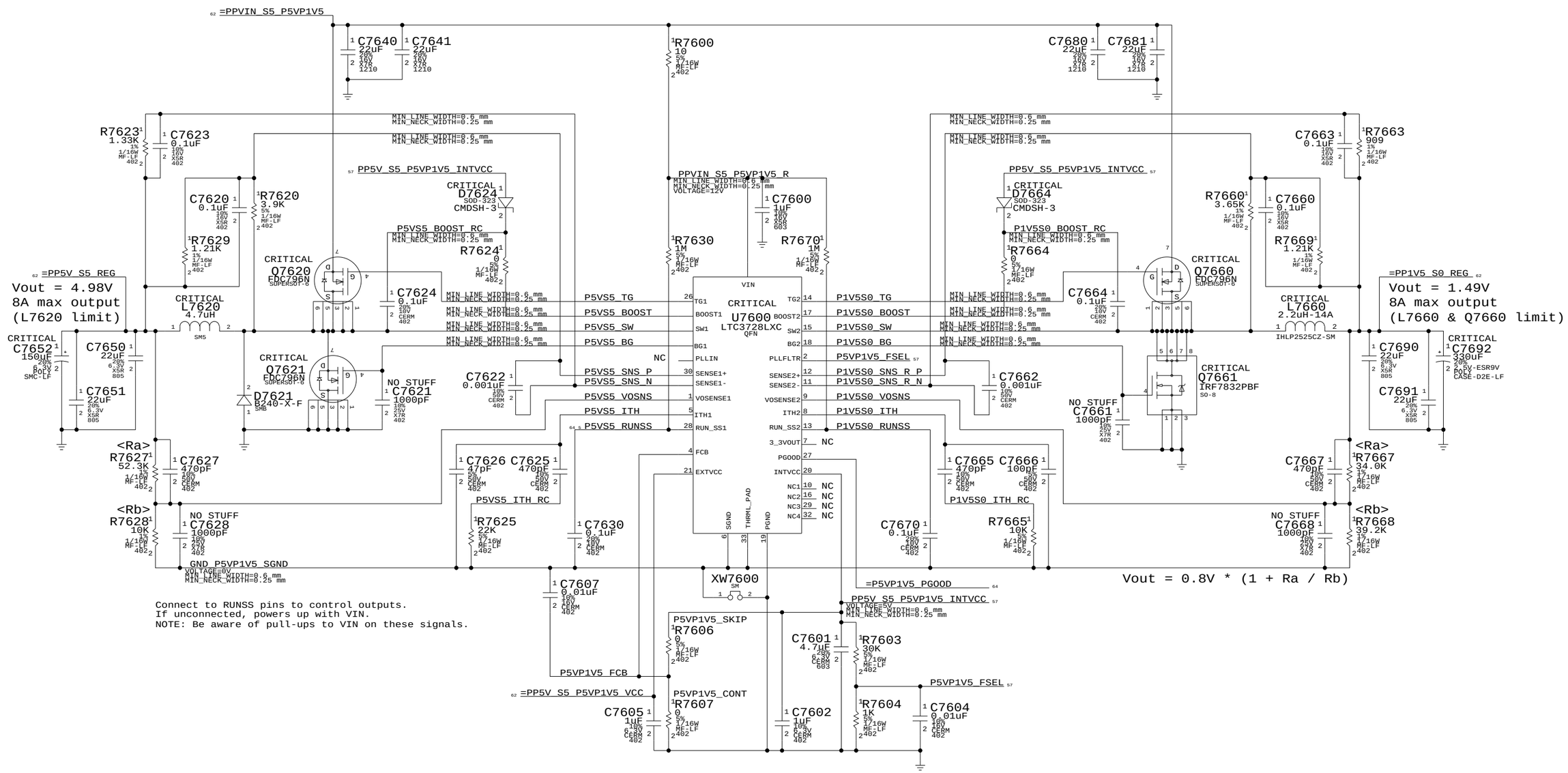

5V / 1.5V Power Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-6941	07001

SCALE	SHT	OF
NONE	57	81

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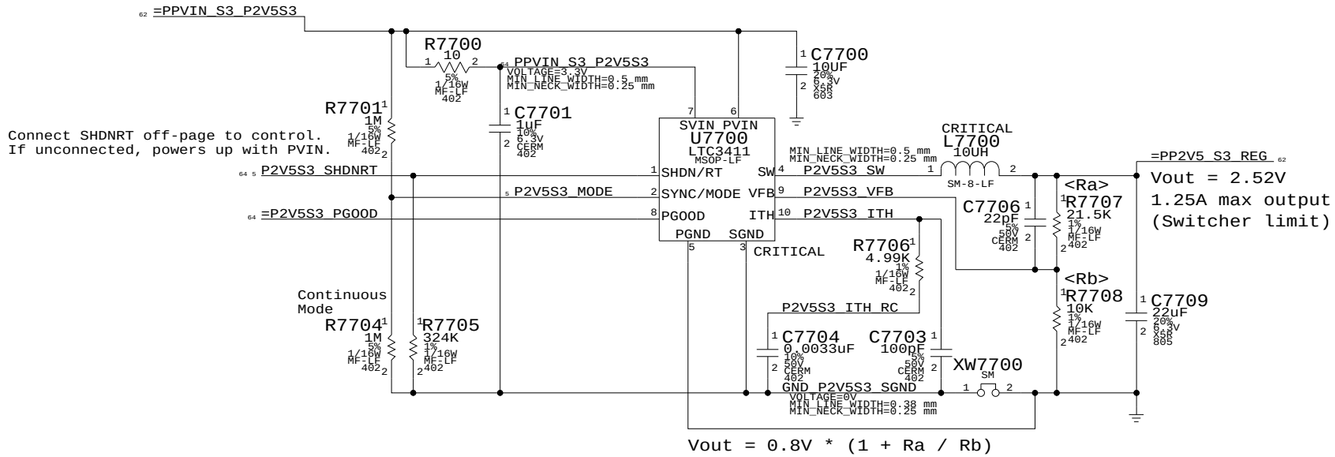
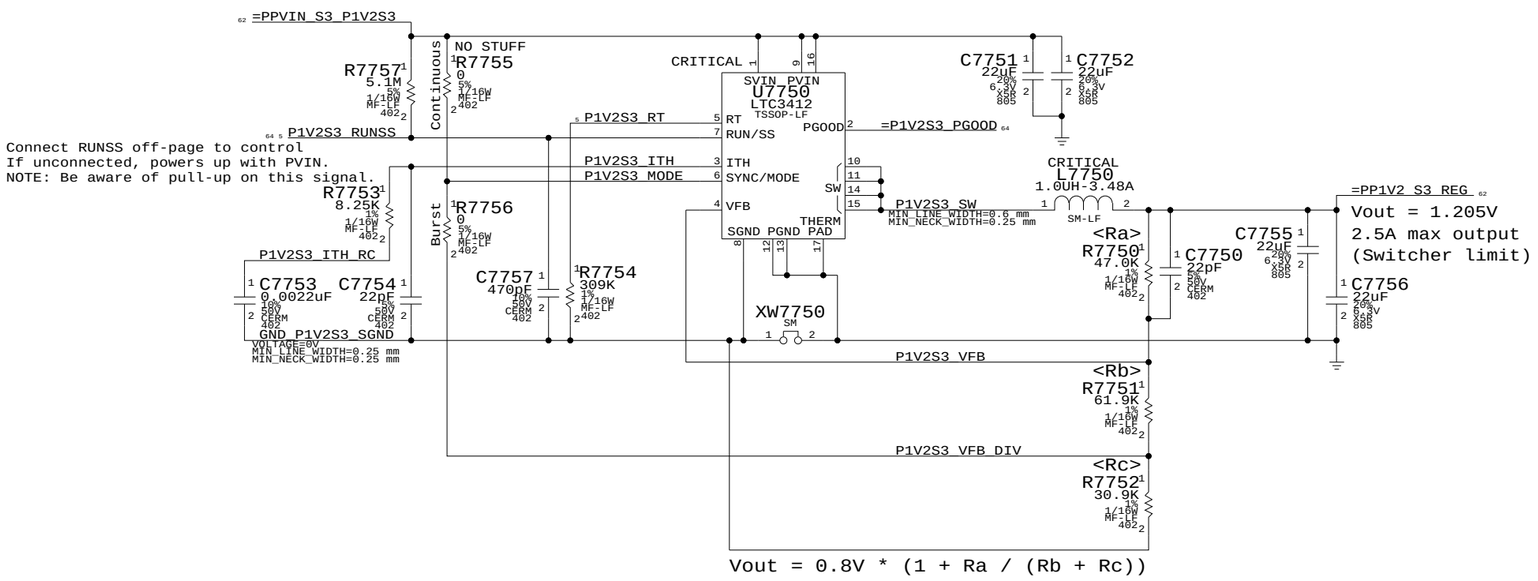
2.5V S3 Regulator



1.2V S3 Regulator



2.5V & 1.2V Regulators

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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	58	81

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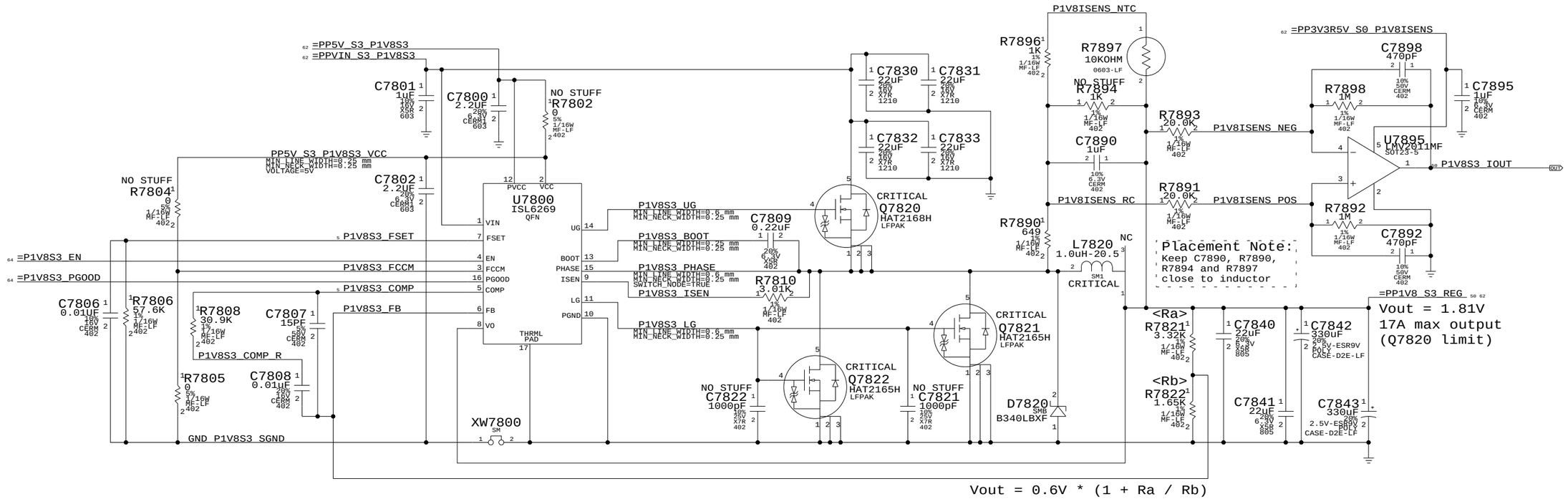
1.8V S3 Current Sense



1.8V Supply

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	D	051-6941	07001
	SCALE: NONE	SHT 59 OF 81	

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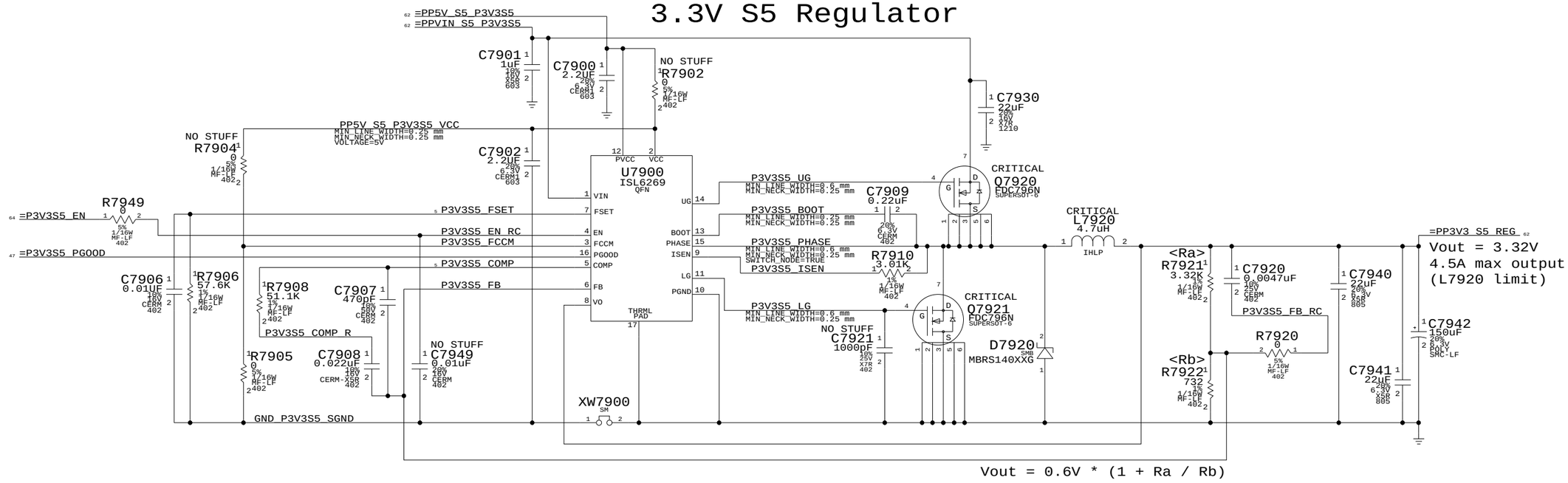
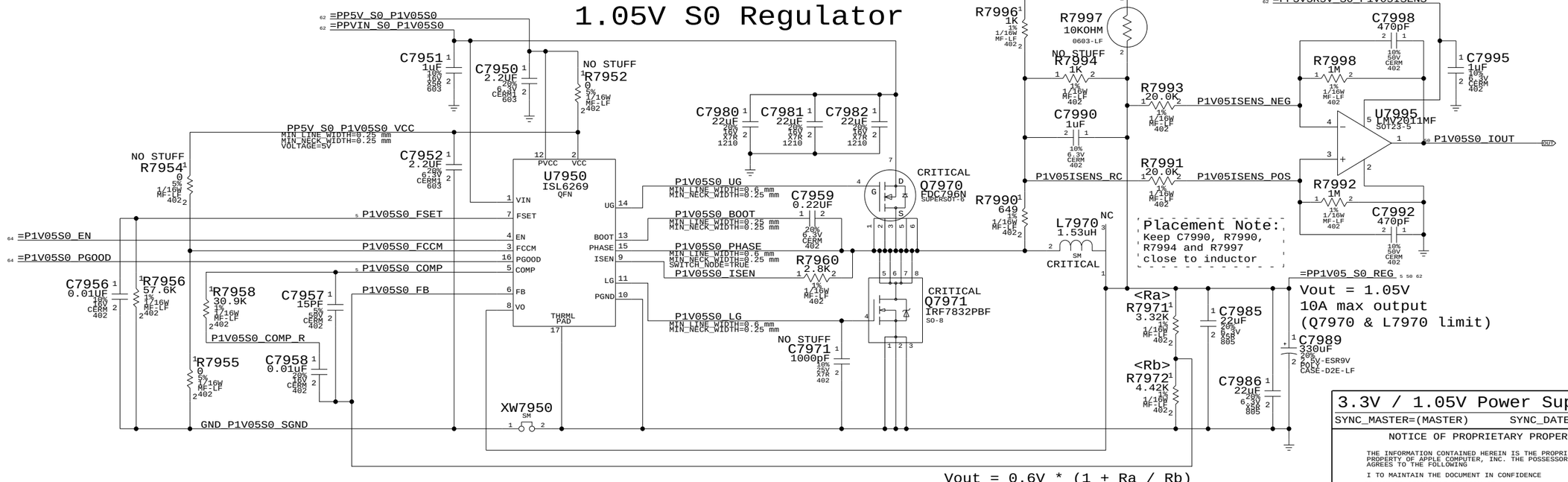
3.3V S5 Regulator


=PP5V_S5_P3V3S5
=PPVIN_S5_P3V3S5
C7901 1uF 10% 16V X5R 603
C7900 2.2UF 20% 6.3V CERM 603
NO STUFF R7902 0 5% 1/16W MF-LF 402
C7930 22uF 20% 16V X7R 1210
PP5V_S5_P3V3S5_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
NO STUFF R7904 0 5% 1/16W MF-LF 402
C7902 2.2UF 20% 6.3V CERM 603
U7900 ISL6269 QFN
PVCC VCC
VIN FSET EN FCCM PGOOD COMP FB VO UG BOOT PHASE ISEN LG PGND THRML PAD
P3V3S5_UG
P3V3S5_BOOT
P3V3S5_PHASE
P3V3S5_ISEN
P3V3S5_LG
C7909 0.22uF 20% 6.3V CERM 402
CRITICAL Q7920 FDC796N SUPERSOT-6
CRITICAL L7920 4.7uH IHLP
=P3V3S5_EN
=P3V3S5_PGOOD
P3V3S5_FSET
P3V3S5_EN_RC
P3V3S5_FCCM
P3V3S5_COMP
P3V3S5_FB
R7949 0 5% 1/16W MF-LF 402
C7906 0.01UF 10% 16V CERM 402
R7906 57.6K 1% 1/16W MF-LF 402
R7908 51.1K 1% 1/16W MF-LF 402
C7907 470PF 10% 50V CERM 402
P3V3S5_COMP_R
R7905 0 5% 1/16W MF-LF 402
C7908 0.022UF 10% 16V CERM-X5R 402
NO STUFF C7949 0.01UF 20% 16V CERM 402
R7910 3.01K 1% 1/16W MF-LF 402
CRITICAL Q7921 FDC796N SUPERSOT-6
NO STUFF C7921 1000PF 10% 25V X7R 402
D7920 SMB MBRS140XXG
<Ra> R7921 3.32K 1% 1/16W MF-LF 402
<Rb> R7922 732 1% 1/16W MF-LF 402
C7920 0.0047uF 10% 25V CERM 402
P3V3S5_FB_RC
R7920 0 5% 1/16W MF-LF 402
C7940 22uF 20% 6.3V X5R 805
C7941 22uF 20% 6.3V X5R 805
=PP3V3_S5_REG
Vout = 3.32V
4.5A max output
(L7920 limit)
C7942 150uF 20% 6.3V POLY SMC-LF
XW7900 SM
GND_P3V3S5_SGND
Vout = 0.6V * (1 + Ra / Rb)

1.05V S0 Regulator


=PP5V_S0_P1V05S0
=PPVIN_S0_P1V05S0
C7951 1uF 10% 16V X5R 603
C7950 2.2UF 20% 6.3V CERM 603
NO STUFF R7952 0 5% 1/16W MF-LF 402
C7980 22uF 20% 16V X7R 1210
C7981 22uF 20% 16V X7R 1210
C7982 22uF 20% 16V X7R 1210
PP5V_S0_P1V05S0_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
NO STUFF R7954 0 5% 1/16W MF-LF 402
C7952 2.2UF 20% 6.3V CERM 603
U7950 ISL6269 QFN
PVCC VCC
VIN FSET EN FCCM PGOOD COMP FB VO UG BOOT PHASE ISEN LG PGND THRML PAD
P1V05S0_UG
P1V05S0_BOOT
P1V05S0_PHASE
P1V05S0_ISEN
P1V05S0_LG
C7959 0.22uF 20% 6.3V CERM 402
CRITICAL Q7970 FDC796N SUPERSOT-6
CRITICAL L7970 1.53uH SM
NC
=P1V05S0_EN
=P1V05S0_PGOOD
P1V05S0_FSET
P1V05S0_FCCM
P1V05S0_COMP
P1V05S0_FB
C7956 0.01UF 10% 16V CERM 402
R7956 57.6K 1% 1/16W MF-LF 402
R7958 30.9K 1% 1/16W MF-LF 402
C7957 15PF 5% 50V CERM 402
P1V05S0_COMP_R
R7955 0 5% 1/16W MF-LF 402
C7958 0.01UF 20% 16V CERM 402
R7960 2.8K 1% 1/16W MF-LF 402
CRITICAL Q7971 IRF7832PBF SO-8
NO STUFF C7971 1000PF 10% 25V X7R 402
P1V05ISENS_NTC
R7996 1K 1% 1/16W MF-LF 402
R7997 10KOHM 0603-LF
NO STUFF R7994 1K 1% 1/16W MF-LF 402
C7990 1uF 10% 6.3V CERM 402
R7993 20.0K 1% 1/16W MF-LF 402
P1V05ISENS_NEG
P1V05ISENS_RC
P1V05ISENS_POS
R7991 20.0K 1% 1/16W MF-LF 402
R7990 649 1% 1/16W MF-LF 402
Placement Note:
Keep C7990, R7990, R7994 and R7997 close to inductor
=PP3V3R5V_S0_P1V05ISENS
C7998 470pF 10% 50V CERM 402
R7998 1M 1% 1/16W MF-LF 402
C7995 1uF 10% 6.3V CERM 402
U7995 LMV2011MF SOT23-5
P1V05S0_IOUT
R7992 1M 1% 1/16W MF-LF 402
C7992 470pF 10% 50V CERM 402
<Ra> R7971 3.32K 1% 1/16W MF-LF 402
<Rb> R7972 4.42K 1% 1/16W MF-LF 402
C7985 22uF 20% 6.3V X5R 805
C7986 22uF 20% 6.3V X5R 805
=PP1V05_S0_REG
Vout = 1.05V
10A max output
(Q7970 & L7970 limit)
C7989 330uF 20% 2V POLY CASE-D2E-LF
XW7950 SM
GND_P1V05S0_SGND
Vout = 0.6V * (1 + Ra / Rb)

1.05V Current Sense

3.3V / 1.05V Power Supplies

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SCALE	SHT	OF
NONE	60	81

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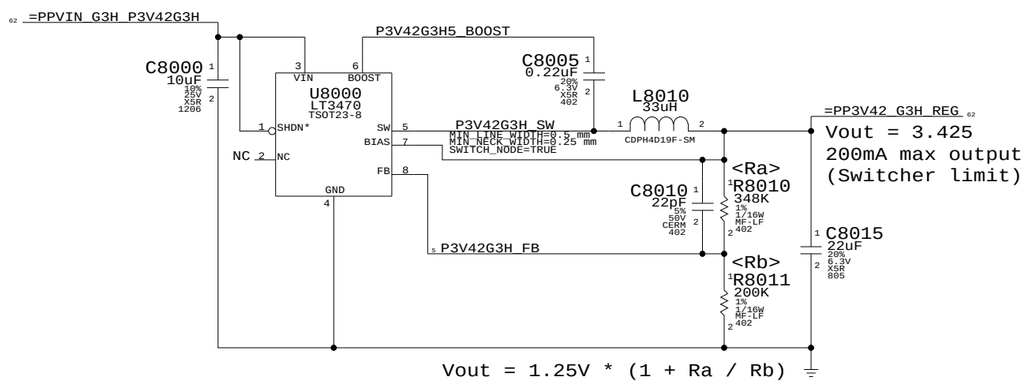
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



3.3V G3Hot Supply

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SCALE	SHT	OF
NONE	61	81

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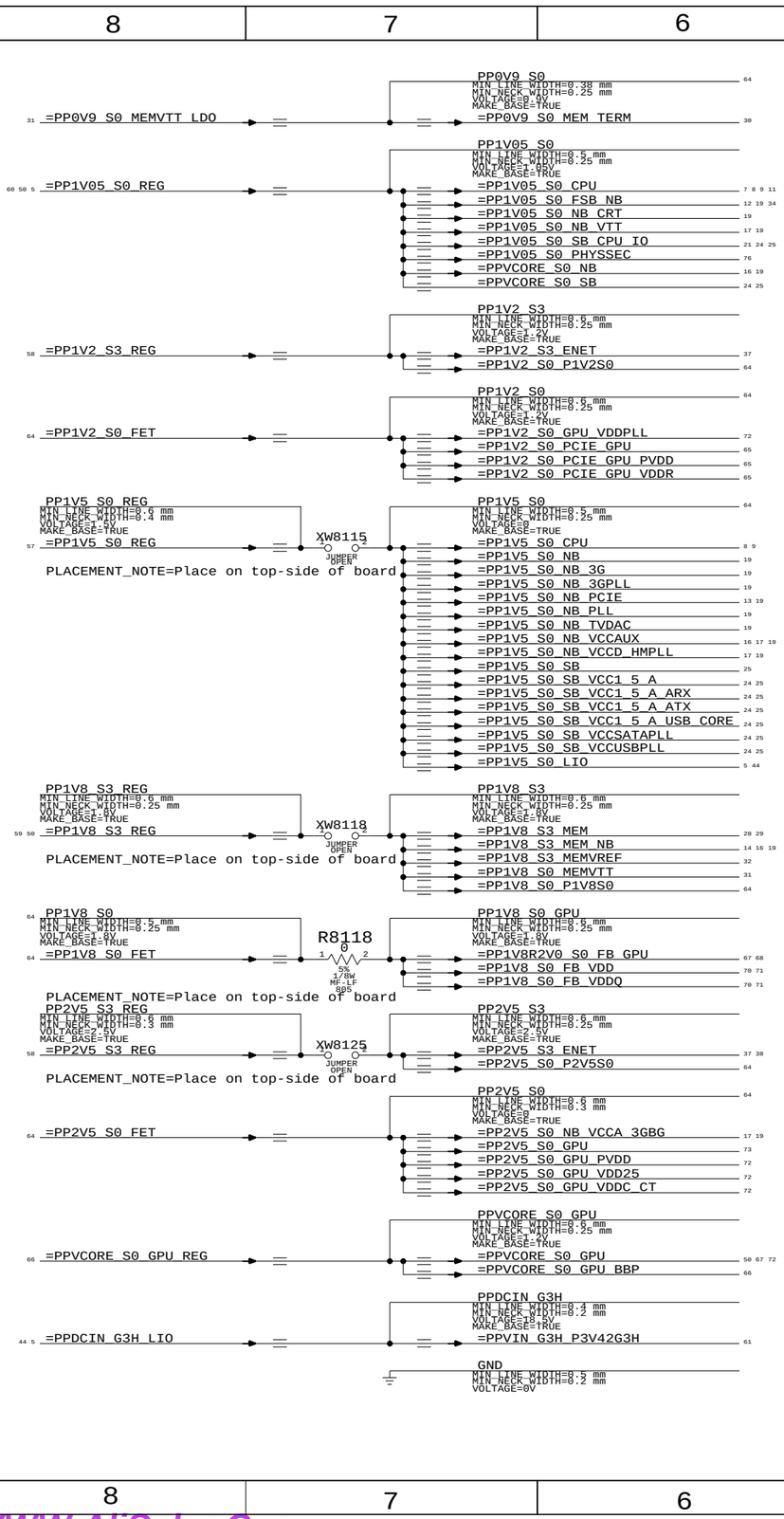

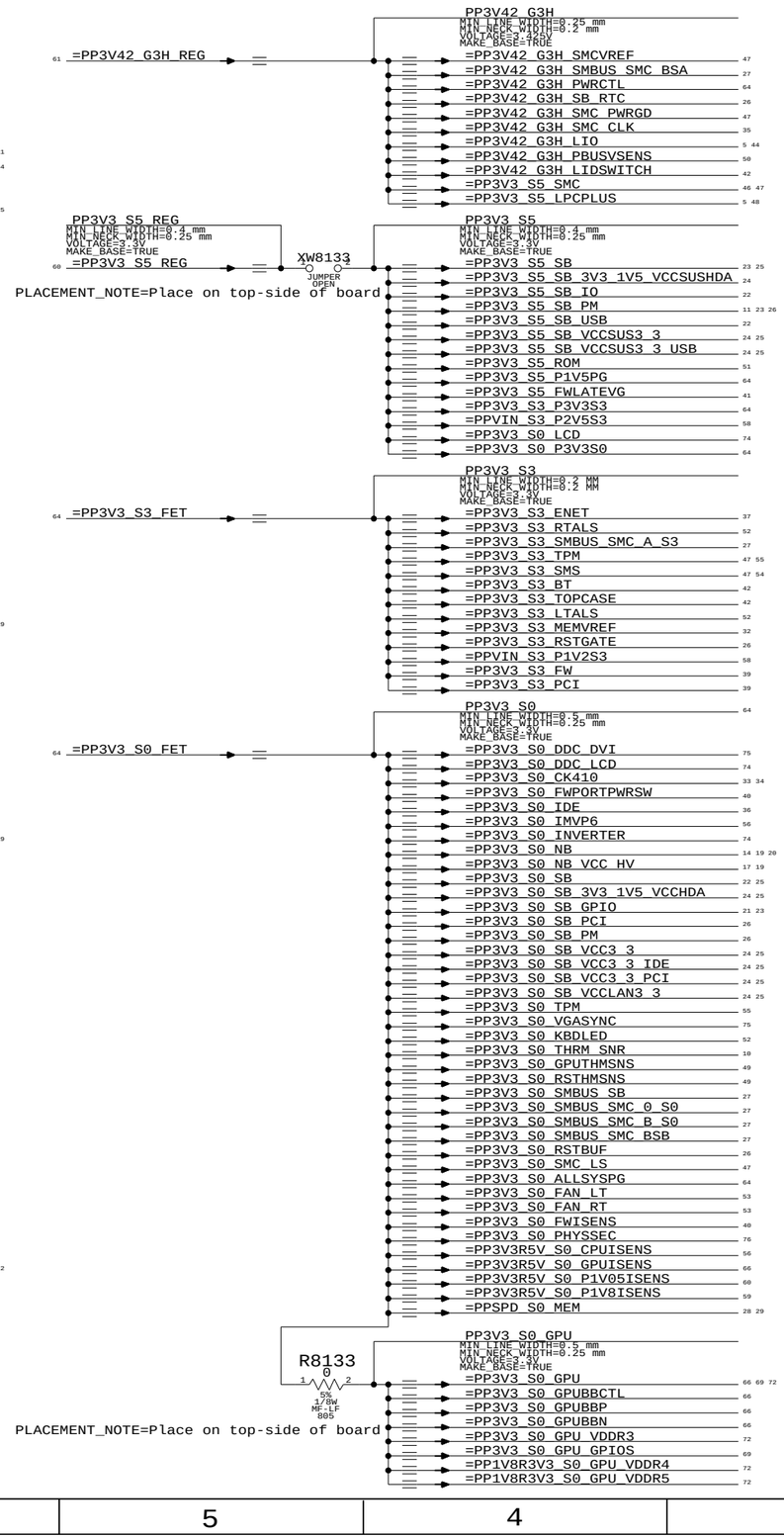

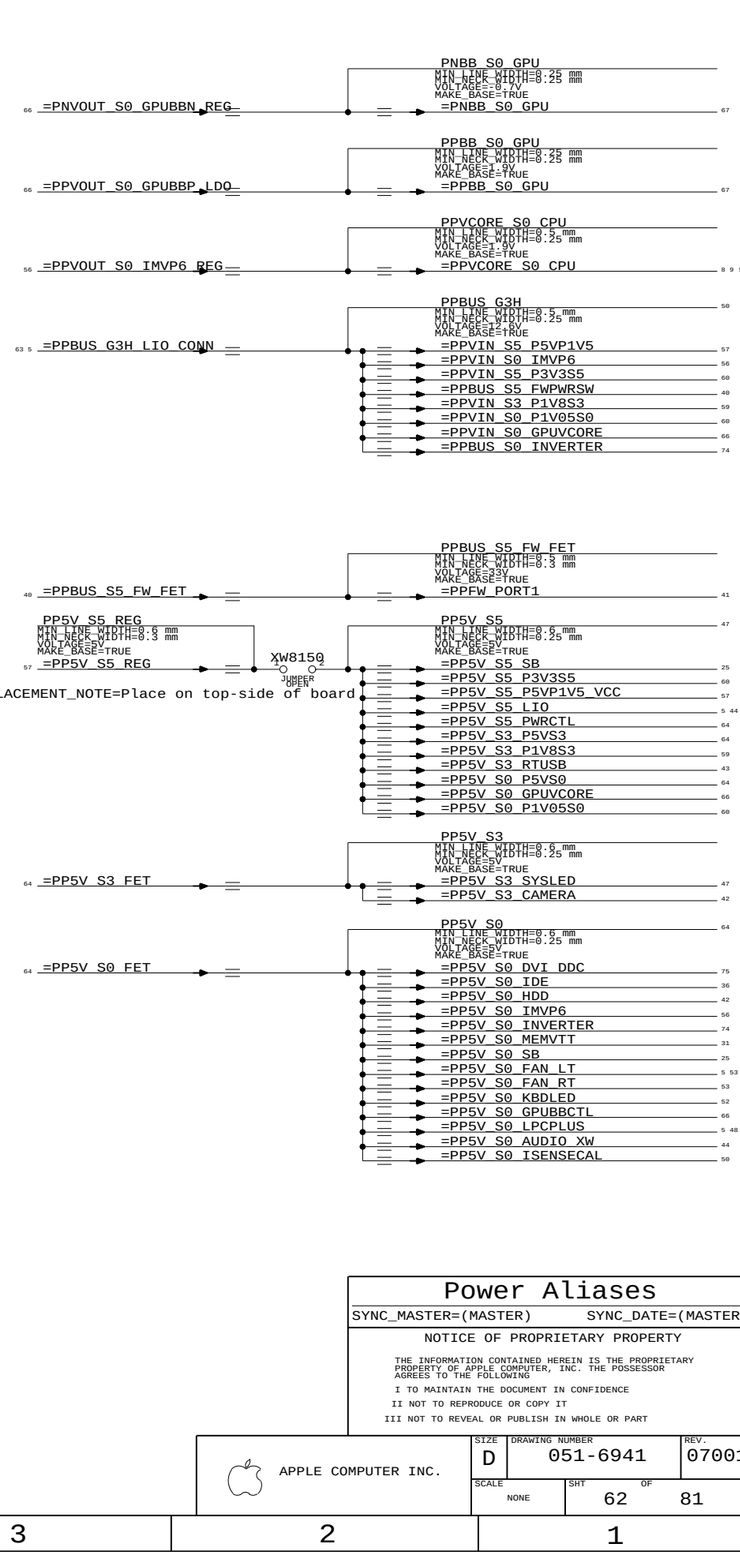

Power Aliases

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SCALE: NONE	SHT: 62 OF: 81	

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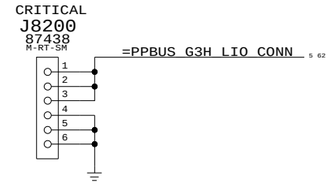
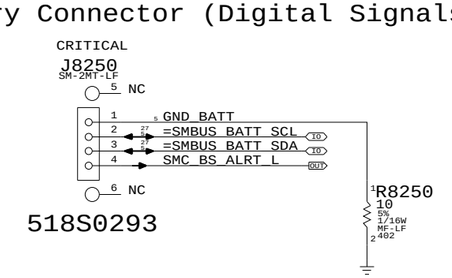
Left I/O Power Connector



518S0368

Battery Connector (Digital Signals)



518S0293

PBus-In & Battery Connectors

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NONE	63	81

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State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Power Control Signals

=PP5V_S5_PWRCTL

R8350 10K 5% 1/16W MF-LF 402

R8351 10K 5% 1/16W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up. (How to guarantee 3.3V?)

=GPUVCORE_PGOOD

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

PM_SLP_S3_LS5V_L (MAKE_BASE=TRUE)

=P2V5S0_EN

=P1V8S0_EN

=P1V2S0_EN

Q8350 2N7002DW-X-F SOT-363

=P5VS0_EN_L

=P3V3S0_EN_L

LIO_P3V3S0_EN_L

=PP3V42_G3H_PWRCTL

PM_SLP_S3_LS5V (MAKE_BASE=TRUE)

Q8350 2N7002DW-X-F SOT-363

R8354 100K 5% 1/16W MF-LF 402

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

Q8357 2N7002DW-X-F SOT-363

PM_SLP_S3_L

PM_SLP_S3

Q8357 2N7002DW-X-F SOT-363

R8356 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) MAKE_BASE=TRUE

=P1V05S0_EN

=GPUVCORE_EN

=MEMVREF_EN

=PBUSVSENS_EN

=PP5V_S5_PWRCTL

R8355 10K 5% 1/16W MF-LF 402

PM_SLP_S4_LS5V (MAKE_BASE=TRUE)

=P5VS3_EN_L

=P3V3S3_EN_L

P1V2S3_RUNSS

1.2V Enable has pull-up to 3.3V

Q8355 2N7002DW-X-F SOT-363

Q8355 2N7002DW-X-F SOT-363

PM_SLP_S4_L

R8357 100K 5% 1/16W MF-LF 402

(PM_SLP_S4_L) MAKE_BASE=TRUE

=P1V8S3_EN

=RTUSB_EN

LIO_P3V3S3_EN

Q8358 TP0610 SOT23-3

PPVIN_S3_P2V5S3

P2V5S3_SHDNRT

2.5V SHDN/RT pin has dual purpose and pull-down at regulator.

=PP3V42_G3H_PWRCTL

P5VS5_PGOOD

(P5VS5_PGOOD) MAKE_BASE=TRUE

=P3V3S5_EN

R8359 470K 5% 1/16W MF-LF 402

P5VS5_RUNSS

5V Enable has pull-up to PBUS

Q8359 2N7002DW-X-F SOT-363

SMC_PM_G2_EN_L

SMC_PM_G2_EN

R8358 100K 5% 1/16W MF-LF 402

Q8359 2N7002DW-X-F SOT-363

5V S3 FET

Q8300 FDC638P SM-LF

=PP5V_S3_P5VS3 → =PP5V_S3_FET

C8300 0.0022uF 10% 50V CERM 402

=P5VS3_EN_L → R8300 0 5% 1/16W MF-LF 402 → P5VS3_EN_L_RC

5V S0 FET

Q8305 FDC638P SM-LF

=PP5V_S0_P5VS0 → =PP5V_S0_FET

C8306 22uF 20% 6.3V X5R 805

C8307 22uF 20% 6.3V X5R 805

C8305 0.0022uF 10% 50V CERM 402

=P5VS0_EN_L → R8305 100K 5% 1/16W MF-LF 402 → P5VS0_EN_L_RC

2.5V S0 FET

Q8320 SI3446DV TSOP-LF

=PP2V5_S0_P2V5S0 → =PP2V5_S0_FET

C8320 0.0022uF 10% 50V CERM 402

=P2V5S0_EN → R8320 0 5% 1/16W MF-LF 402 → P2V5S0_EN_RC

3.3V S3 FET

Q8310 FDC638P SM-LF

=PP3V3_S3_P3V3S3 → =PP3V3_S3_FET

C8310 0.0022uF 10% 50V CERM 402

=P3V3S3_EN_L → R8310 100K 5% 1/16W MF-LF 402 → P3V3S3_EN_L_RC

3.3V S0 FET

Q8315 FDC638P SM-LF

=PP3V3_S0_P3V3S0 → =PP3V3_S0_FET

C8315 0.0022uF 10% 50V CERM 402

=P3V3S0_EN_L → R8315 100K 5% 1/16W MF-LF 402 → P3V3S0_EN_L_RC

1.8V S0 FET

Q8325 FDC796N SUPERSOT-6

=PP1V8_S0_P1V8S0 → =PP1V8_S0_FET

C8325 0.0022uF 10% 50V CERM 402

C8326 22uF 20% 6.3V X5R 805

C8327 22uF 20% 6.3V X5R 805

=P1V8S0_EN → R8325 0 5% 1/16W MF-LF 402 → P1V8S0_EN_RC

1.2V S0 FET

Q8330 SI3446DV TSOP-LF

=PP1V2_S0_P1V2S0 → =PP1V2_S0_FET

C8330 0.0022uF 10% 50V CERM 402

=P1V2S0_EN → R8330 0 5% 1/16W MF-LF 402 → P1V2S0_EN_RC

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

=PP3V3_S5_P1V5PG

PP1V5_S0

R8361 27.4K 1% 1/16W MF-LF 402

R8363 4.99K 1% 1/16W MF-LF 402

C8360 0.1uF 20% 10V CERM 402

0.89V Reference

U8360 LMC7211 SM-LF

P1V0_P1V5PG_REF

P1V5S0_COMP_POS

P1V5S0_PGOOD

R8362 10K 1% 1/16W MF-LF 402

R8364 10K 1% 1/16W MF-LF 402

R8365 10K 5% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

IMVP_PWRGD_IN

=P1V05S0_PGOOD

P1V5P1V05S0_PGOOD (MAKE_BASE=TRUE)

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)

NOTE: R8365 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

=P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)

=P2V5S3_PGOOD — TP_P2V5S3_PGOOD (MAKE_BASE=TRUE)

=P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

=P1V2S3_PGOOD — TP_P1V2S3_PGOOD (MAKE_BASE=TRUE)

These rails are monitored by LTC2908

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

PP5V_S0

PP3V3_S0

PP2V5_S0

PP1V8_S0

PP1V2_S0

PP0V9_S0

C8370 0.1uF 20% 10V CERM 402

C8371 0.1uF 20% 10V CERM 402

R8374 68.1K 1% 1/16W MF-LF 402

R8372 124K 1% 1/16W MF-LF 402

U8370 LTC2908 LLP

V3, V4 CRITICAL, VADJ1, VADJ2, GND, V1, V2, RST*, THRML PAD

S0PGOOD_1V2_DIV

S0PGOOD_0V9_DIV

S0PGOOD_PWROK

R8375 100K 1% 1/16W MF-LF 402

R8373 100K 1% 1/16W MF-LF 402

R8376 549K 1% 1/16W MF-LF 402

LTC2908 sources 6uA at 5.0V R8375 serves as pull-down and 3.3V level-shifter.

LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)

=PP3V3_S0_ALLSYSPG

U8380 MC74VHC1G08 SC70

ALL_SYS_PWRGD

C8380 0.1UF 20% 10V CERM 402

S3/S0 FETs & Power Control

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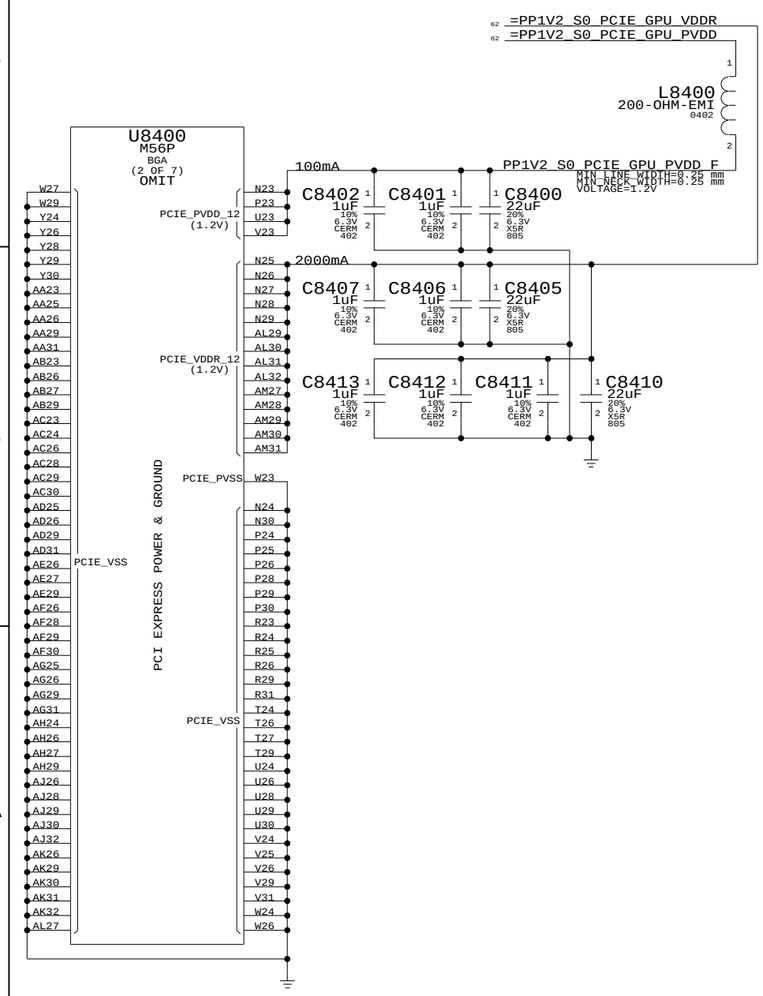
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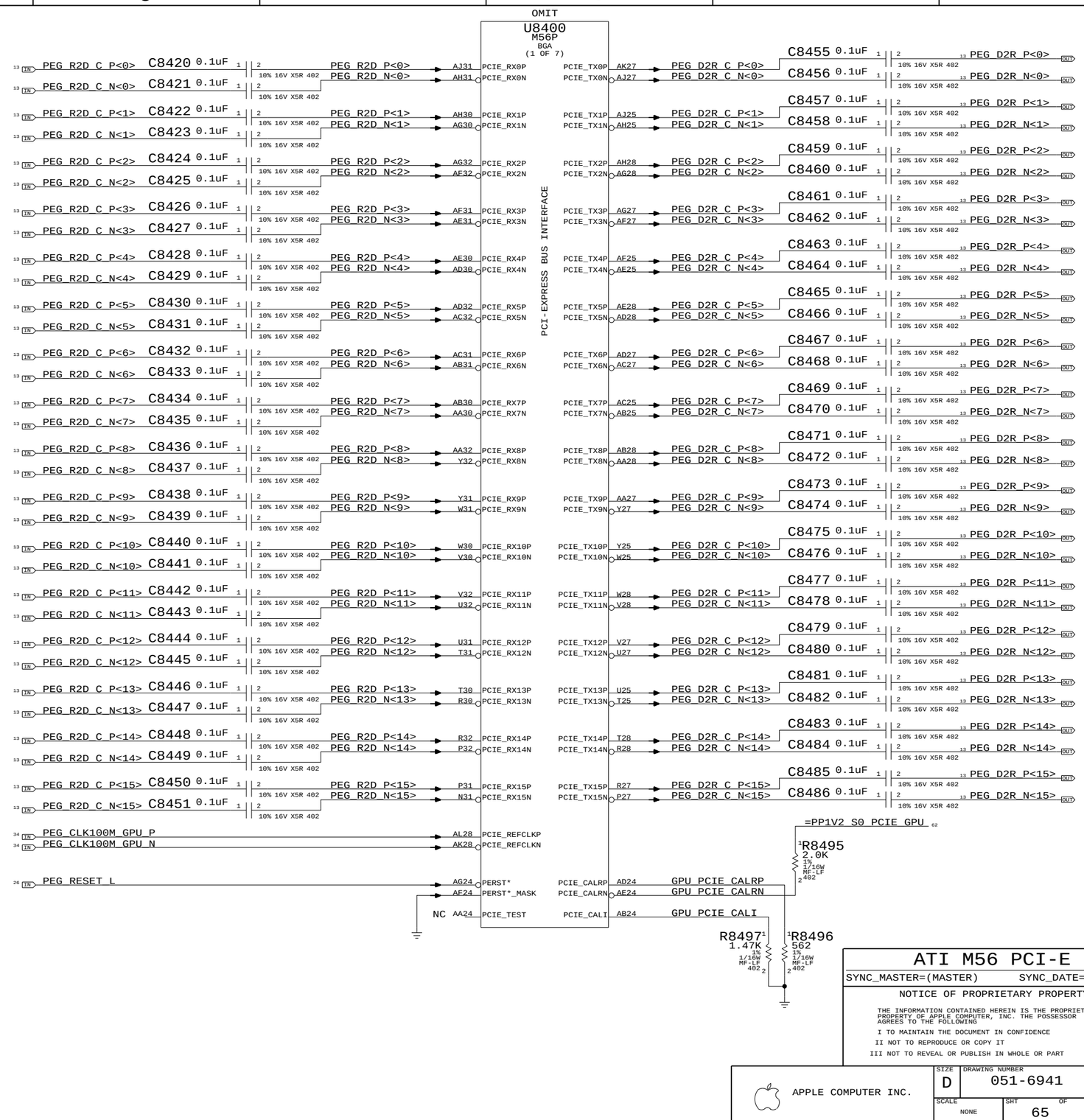
L8400
200-OHM-EMI
0402
U8400
M56P
BGA
(2 OF 7)
OMIT
100mA
PP1V2_S0_PCIE_GPU_PVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
PCIE_PVDD_12 (1.2V)
C8402 1uF 10% 6.3V CERM 402
C8401 1uF 10% 6.3V CERM 402
C8400 22uF 20% 6.3V X5R 805
2000mA
C8407 1uF 10% 6.3V CERM 402
C8406 1uF 10% 6.3V CERM 402
C8405 22uF 20% 6.3V X5R 805
PCIE_VDDR_12 (1.2V)
C8413 1uF 10% 6.3V CERM 402
C8412 1uF 10% 6.3V CERM 402
C8411 1uF 10% 6.3V CERM 402
C8410 22uF 20% 6.3V X5R 805
PCIE_PVSS
PCIE_VSS
PCIE_VSS
PCI EXPRESS POWER & GROUND
W27 W29 Y24 Y26 Y28 Y29 Y30 AA23 AA25 AA26 AA29 AA31 AB23 AB26 AB27 AB29 AC23 AC24 AC26 AC28 AC29 AC30 AD25 AD26 AD29 AD31 AE26 AE27 AE29 AE26 AE28 AF29 AF30 AG25 AG26 AG29 AG31 AH24 AH26 AH27 AH29 AJ26 AJ28 AJ29 AJ30 AJ32 AK26 AK29 AK30 AK31 AK32 AL27
N23 P23 U23 V23 N25 N26 N27 N28 N29 AL29 AL30 AL31 AL32 AM27 AM28 AM29 AM30 AM31 W23 N24 N30 P24 P25 P26 P28 P29 P30 R23 R24 R25 R26 R29 R31 T24 T26 T27 T29 U24 U26 U28 U29 U30 V24 V25 V26 V29 V31 W24 W26


OMIT
U8400
M56P
BGA
(1 OF 7)
PCI-EXPRESS BUS INTERFACE
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PEG_R2D_C_N<2> C8425 0.1uF PEG_R2D_N<2> AF32 PCIE_RX2N
PEG_R2D_C_P<3> C8426 0.1uF PEG_R2D_P<3> AF31 PCIE_RX3P
PEG_R2D_C_N<3> C8427 0.1uF PEG_R2D_N<3> AE31 PCIE_RX3N
PEG_R2D_C_P<4> C8428 0.1uF PEG_R2D_P<4> AE30 PCIE_RX4P
PEG_R2D_C_N<4> C8429 0.1uF PEG_R2D_N<4> AD30 PCIE_RX4N
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PEG_R2D_C_P<6> C8432 0.1uF PEG_R2D_P<6> AC31 PCIE_RX6P
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PEG_R2D_C_N<11> C8443 0.1uF PEG_R2D_N<11> U32 PCIE_RX11N
PEG_R2D_C_P<12> C8444 0.1uF PEG_R2D_P<12> U31 PCIE_RX12P
PEG_R2D_C_N<12> C8445 0.1uF PEG_R2D_N<12> T31 PCIE_RX12N
PEG_R2D_C_P<13> C8446 0.1uF PEG_R2D_P<13> T30 PCIE_RX13P
PEG_R2D_C_N<13> C8447 0.1uF PEG_R2D_N<13> R30 PCIE_RX13N
PEG_R2D_C_P<14> C8448 0.1uF PEG_R2D_P<14> R32 PCIE_RX14P
PEG_R2D_C_N<14> C8449 0.1uF PEG_R2D_N<14> P32 PCIE_RX14N
PEG_R2D_C_P<15> C8450 0.1uF PEG_R2D_P<15> P31 PCIE_RX15P
PEG_R2D_C_N<15> C8451 0.1uF PEG_R2D_N<15> N31 PCIE_RX15N
PEG_CLK100M_GPU_P AL28 PCIE_REFCLKP
PEG_CLK100M_GPU_N AK28 PCIE_REFCLKN
PEG_RESET_L AG24 PERST*
AF24 PERST*_MASK
NC AA24 PCIE_TEST
PCIE_TX0P AK27 PEG_D2R_C_P<0> C8455 0.1uF PEG_D2R_P<0>
PCIE_TX0N AJ27 PEG_D2R_C_N<0> C8456 0.1uF PEG_D2R_N<0>
PCIE_TX1P AJ25 PEG_D2R_C_P<1> C8457 0.1uF PEG_D2R_P<1>
PCIE_TX1N AH25 PEG_D2R_C_N<1> C8458 0.1uF PEG_D2R_N<1>
PCIE_TX2P AH28 PEG_D2R_C_P<2> C8459 0.1uF PEG_D2R_P<2>
PCIE_TX2N AG28 PEG_D2R_C_N<2> C8460 0.1uF PEG_D2R_N<2>
PCIE_TX3P AG27 PEG_D2R_C_P<3> C8461 0.1uF PEG_D2R_P<3>
PCIE_TX3N AF27 PEG_D2R_C_N<3> C8462 0.1uF PEG_D2R_N<3>
PCIE_TX4P AF25 PEG_D2R_C_P<4> C8463 0.1uF PEG_D2R_P<4>
PCIE_TX4N AE25 PEG_D2R_C_N<4> C8464 0.1uF PEG_D2R_N<4>
PCIE_TX5P AE28 PEG_D2R_C_P<5> C8465 0.1uF PEG_D2R_P<5>
PCIE_TX5N AD28 PEG_D2R_C_N<5> C8466 0.1uF PEG_D2R_N<5>
PCIE_TX6P AD27 PEG_D2R_C_P<6> C8467 0.1uF PEG_D2R_P<6>
PCIE_TX6N AC27 PEG_D2R_C_N<6> C8468 0.1uF PEG_D2R_N<6>
PCIE_TX7P AC25 PEG_D2R_C_P<7> C8469 0.1uF PEG_D2R_P<7>
PCIE_TX7N AB25 PEG_D2R_C_N<7> C8470 0.1uF PEG_D2R_N<7>
PCIE_TX8P AB28 PEG_D2R_C_P<8> C8471 0.1uF PEG_D2R_P<8>
PCIE_TX8N AA28 PEG_D2R_C_N<8> C8472 0.1uF PEG_D2R_N<8>
PCIE_TX9P AA27 PEG_D2R_C_P<9> C8473 0.1uF PEG_D2R_P<9>
PCIE_TX9N Y27 PEG_D2R_C_N<9> C8474 0.1uF PEG_D2R_N<9>
PCIE_TX10P Y25 PEG_D2R_C_P<10> C8475 0.1uF PEG_D2R_P<10>
PCIE_TX10N W25 PEG_D2R_C_N<10> C8476 0.1uF PEG_D2R_N<10>
PCIE_TX11P W28 PEG_D2R_C_P<11> C8477 0.1uF PEG_D2R_P<11>
PCIE_TX11N V28 PEG_D2R_C_N<11> C8478 0.1uF PEG_D2R_N<11>
PCIE_TX12P V27 PEG_D2R_C_P<12> C8479 0.1uF PEG_D2R_P<12>
PCIE_TX12N U27 PEG_D2R_C_N<12> C8480 0.1uF PEG_D2R_N<12>
PCIE_TX13P U25 PEG_D2R_C_P<13> C8481 0.1uF PEG_D2R_P<13>
PCIE_TX13N T25 PEG_D2R_C_N<13> C8482 0.1uF PEG_D2R_N<13>
PCIE_TX14P T28 PEG_D2R_C_P<14> C8483 0.1uF PEG_D2R_P<14>
PCIE_TX14N R28 PEG_D2R_C_N<14> C8484 0.1uF PEG_D2R_N<14>
PCIE_TX15P R27 PEG_D2R_C_P<15> C8485 0.1uF PEG_D2R_P<15>
PCIE_TX15N P27 PEG_D2R_C_N<15> C8486 0.1uF PEG_D2R_N<15>
PCIE_CALRP AD24 GPU_PCIE_CALRP
PCIE_CALRN AE24 GPU_PCIE_CALRN
PCIE_CALI AB24 GPU_PCIE_CALI
=PP1V2_S0_PCIE_GPU 62
R8495 2.0K 1% 1/16W MF-LF 402
R8497 1.47K 1% 1/10W MF-LF 402
R8496 562 1% 1/16W MF-LF 402
10% 16V X5R 402
OUT
IN

ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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GPU VCore Current Sense

GPU VCore Supply

=PP5V_S0_GPUVCORE
=PPVIN_S0_GPUVCORE
C8501 1uF 10% 16V X5R 603
C8500 2.2UF 20% 6.3V CERM 603
NO STUFF R8502 0 5% 1/16W MF-LF 402
PP5V_S0_GPUVCORE_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
C8502 2.2UF 20% 6.3V CERM 603
NO STUFF R8504 0 5% 1/16W MF-LF 402
U8500 ISL6269 QFN
PVCC VCC VIN FSET EN FCCM PGOOD COMP FB VO UG BOOT PHASE ISEN LG PGND THRML PAD
=GPUVCORE_EN
=GPUVCORE_PGOOD
GPUVCORE_FSET
GPUVCORE_FCCM
GPUVCORE_COMP
GPUVCORE_FB
GPUVCORE_UG
GPUVCORE_BOOT
GPUVCORE_PHASE
GPUVCORE_ISEN
GPUVCORE_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
C8509 0.22UF 20% 6.3V CERM 402
R8510 3.01K 1% 1/16W MF-LF 402
C8530 22uF 20% 16V X7R 1210
C8531 22uF 20% 16V X7R 1210
C8532 22uF 20% 16V X7R 1210
CRITICAL Q8520 HAT2168H LFPAK
CRITICAL Q8521 HAT2165H LFPAK
CRITICAL Q8522 HAT2165H LFPAK
CRITICAL L8520 1.0uH-20.5 SM1
NC
R8508 51.1K 1% 1/16W MF-LF 402
C8507 470pF 10% 50V CERM 402
GPUVCORE_COMP_R
C8506 0.01UF 10% 16V CERM 402
R8506 57.6K 1% 1/16W MF-LF 402
R8505 0 5% 1/16W MF-LF 402
C8508 0.022UF 10% 16V CERM-X5R 402
GND_GPUVCORE_SGND
XW8500 SM
NO STUFF C8522 1000pF 10% 25V X7R 402
NO STUFF C8521 1000pF 10% 25V X7R 402
D8520 B340LBXF
R8596 1K 1% 1/10W MF-LF 402
R8597 10KOHM 0603-LF
NO STUFF R8594 1K 1% 1/10W MF-LF 402
C8590 1uF 10% 6.3V CERM 402
R8593 20.0K 1% 1/10W MF-LF 402
GPUISENS_NEG
GPUISENS_RC
R8591 20.0K 1% 1/10W MF-LF 402
GPUISENS_POS
R8590 649 1% 1/10W MF-LF 402
GPUISENS_NTC
=PP3V3R5V_S0_GPUISENS
C8598 470pF 10% 50V CERM 402
R8598 1M 1% 1/16W MF-LF 402
C8595 1uF 10% 6.3V CERM 402
U8595 LMV2011MF SOT23-5
GPUVCORE_IOUT
R8592 1M 1% 1/16W MF-LF 402
C8592 470pF 10% 50V CERM 402
Placement Note:
Keep C8590, R8590, R8594 and R8597 close to inductor
=PPVCORE_S0_GPU_REG
Vout = 1.08V / 1.00V
17A max output
(Q8520 limit)
<Ra> R8521 10K 1% 1/16W MF-LF 402
<Rb> R8522 15.0K 1% 1/16W MF-LF 402
<Rc> R8523 75K 1% 1/16W MF-LF 402
C8520 0.0047uF 10% 25V CERM 402
C8540 22uF 20% 6.3V X5R 805
C8541 22uF 20% 6.3V X5R 805
C8542 330uF 20% 2.5V-ESR9V CASE-D2E-LF
C8543 330uF 20% 2.5V-ESR9V CASE-D2E-LF
GPUVCORE_FB_LOW

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

=PPVCORE_S0_GPU_BBP
Q8575 FDC796N SUPERSOT-6 CRITICAL
GPUBB_EN_L
=PPVOUT_S0_GPUBBP_LDO
Vout = 1.58V / 1.50V
180mA max output
(LDO limit)
=PP3V3_S0_GPUBBP
U8550 FAN2558 SOT23-6-LF CRITICAL
VIN PG EN VOUT ADJ GND
GPUBB_EN
C8551 2.2uF 20% 6.3V CERM 603
C8555 0.01UF 10% 16V CERM 402
<Ra> R8555 24.9K 1% 1/16W MF-LF 402
C8556 22uF 20% 6.3V X5R 805
GPUBBP_ADJ
<Rc> R8554 174K 1% 1/16W MF-LF 402
<Rb> R8556 16.2K 1% 1/16W MF-LF 402
C8557 22uF 20% 6.3V X5R 805
GPUBBP_ADJ_LOW
Q8554 2N7002 SOT23-LF
GPU_VCORE_HIGH

Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
=PP5V_S0_GPUBBCTL
FDC796N max Vgs is 3.0V
Vin must be > 4.2V
R8570 100K 5% 1/16W MF-LF 402
=PP3V3_S0_GPUBBCTL
GPU_BB_CTL
R8561 0 5% 1/16W MF-LF 402
GPU_GENERICD
GPU_BB_EN
U8560 MC74VHC1G08 SC70
GPUBB_EN
GPUBB_EN_L
R8560 10K 5% 1/16W MF-LF 402
C8560 1UF 10% 6.3V CERM 402
Q8570 2N7002 SOT23-LF
C8570 0.01uF 10% 16V CERM 402

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active.
When inactive, provides VSS to BBN pins.

=PP3V3_S0_GPUBBN
C8580 10uF 20% 6.3V X5R 603
CRITICAL L8585 15uH SDQ12150-SM
GPUBBN_SW
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
GPUBBN_D
C8585 330pF 10% 50V CERM 402
GPUBBN_D_RC
R8585 10 5% 1/16W MF-LF 603
C8589 22uF 20% 6.3V X5R 805
=PNVOUT_S0_GPUBBN_REG
Vout = -0.50V
150mA max output
(Inductor & IC current limit)
Q8576 FDC796N SUPERSOT-6 CRITICAL
GPUBB_EN_L
Watch FET Vgs, since Vs will be negative
FDC796N min Vgs is 1.0V
U8580 LT3483 TSOT23-6 CRITICAL
SW VIN SHDN* GND FB (GPUBBN_D)
GPUBB_EN
GPUBBN_FB
C8586 220pF 5% 25V CERM 402
<Ra> R8586 49.9K 1% 1/16W MF-LF 402

Vout = -10uA * Ra

GPU (M56) Core Supplies		
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	SCALE NONE	SHT 66 OF 81

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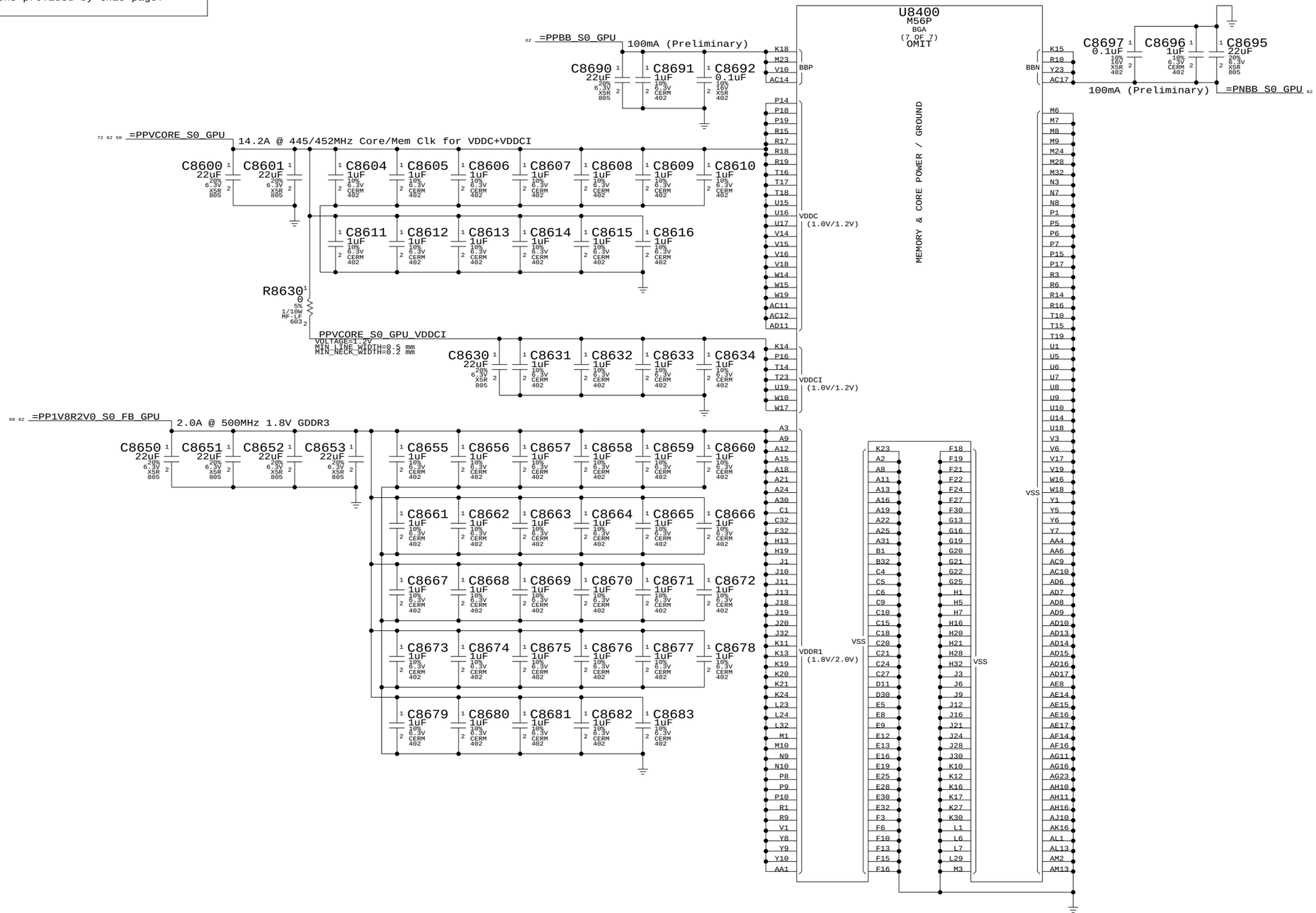
Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

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Page Notes

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- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
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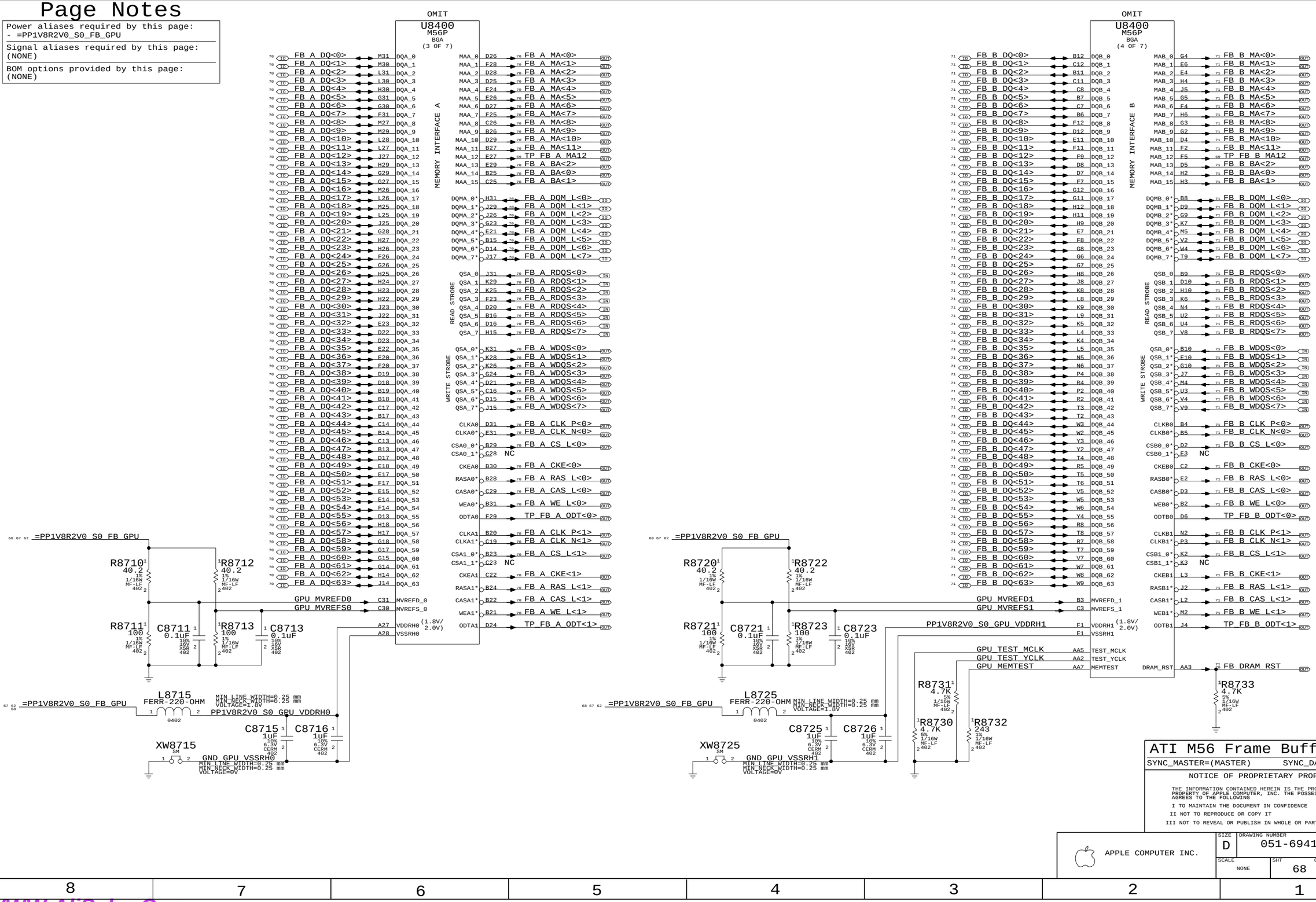

ATI M56 Frame Buffer I/F

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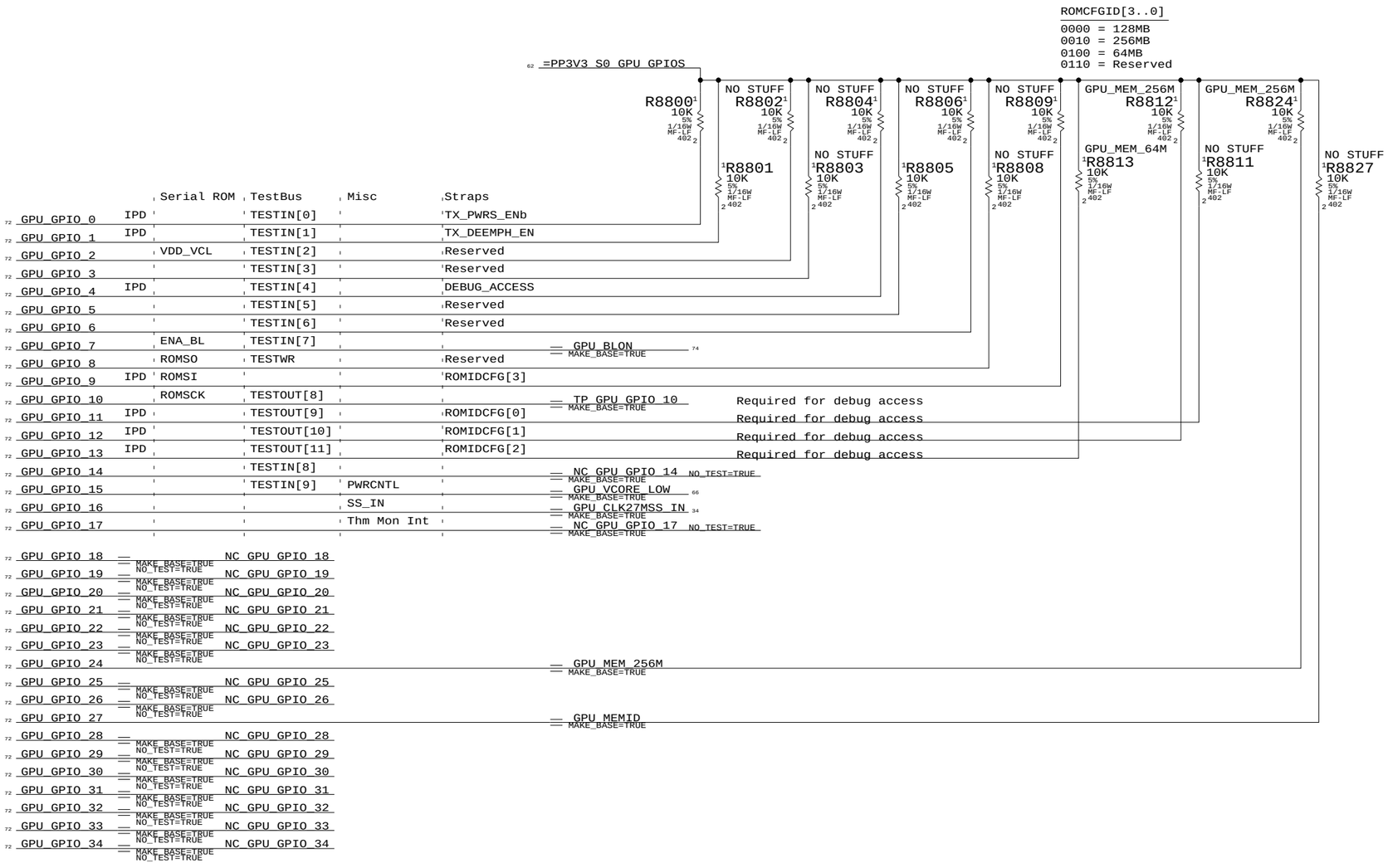

Renamed signals

GPU_CLK27M (MAKE_BASE=TRUE) — GPU_XTALIN

Unused signals

NC_GPU_XTALOUT (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_XTALOUT
NC_ATI_ROMCS_L (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_ATI_ROMCS_L
NC_FB_A_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_A_MA12
NC_FB_B_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_B_MA12
NC_GPU_GENERICA (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICA
NC_GPU_GENERICB (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICB
NC_GPU_GENERICC (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICC
NC_GPU_VGA_R (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_R
NC_GPU_VGA_G (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_G
NC_GPU_VGA_B (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_B
TP_GPU_VGA_HSYNC (MAKE_BASE=TRUE)		GPU_VGA_HSYNC
TP_GPU_VGA_VSYNC (MAKE_BASE=TRUE)		GPU_VGA_VSYNC
NC_GPU_TV_Y (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_Y
NC_GPU_TV_C (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_C
NC_GPU_TV_COMP (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_COMP
NC_LVDS_U_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_P<3>
NC_LVDS_U_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_N<3>
NC_LVDS_L_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_P<3>
NC_LVDS_L_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_N<3>
NC_ATI_DVPCLK (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCLK
NC_ATI_DVPCNTL<2..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCNTL<2..0>
NC_ATI_DVPDATA<15..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPDATA<15..0>

Required for debug access

TP_ATI_DVPDATA<23..16> (MAKE_BASE=TRUE) — ATI_DVPDATA<23..16>

Also required: GPIO10 - GPIO13

=PP3V3_S0_GPU

R9390 4.7K 5% 1/16W MF-LF 402
R9391 4.7K 5% 1/16W MF-LF 402

GPU_DDC_B_CLK
GPU_DDC_B_DATA

GPU Straps

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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

Connect to designated pin, then GND

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_MASTER=(MASTER)

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Page Notes

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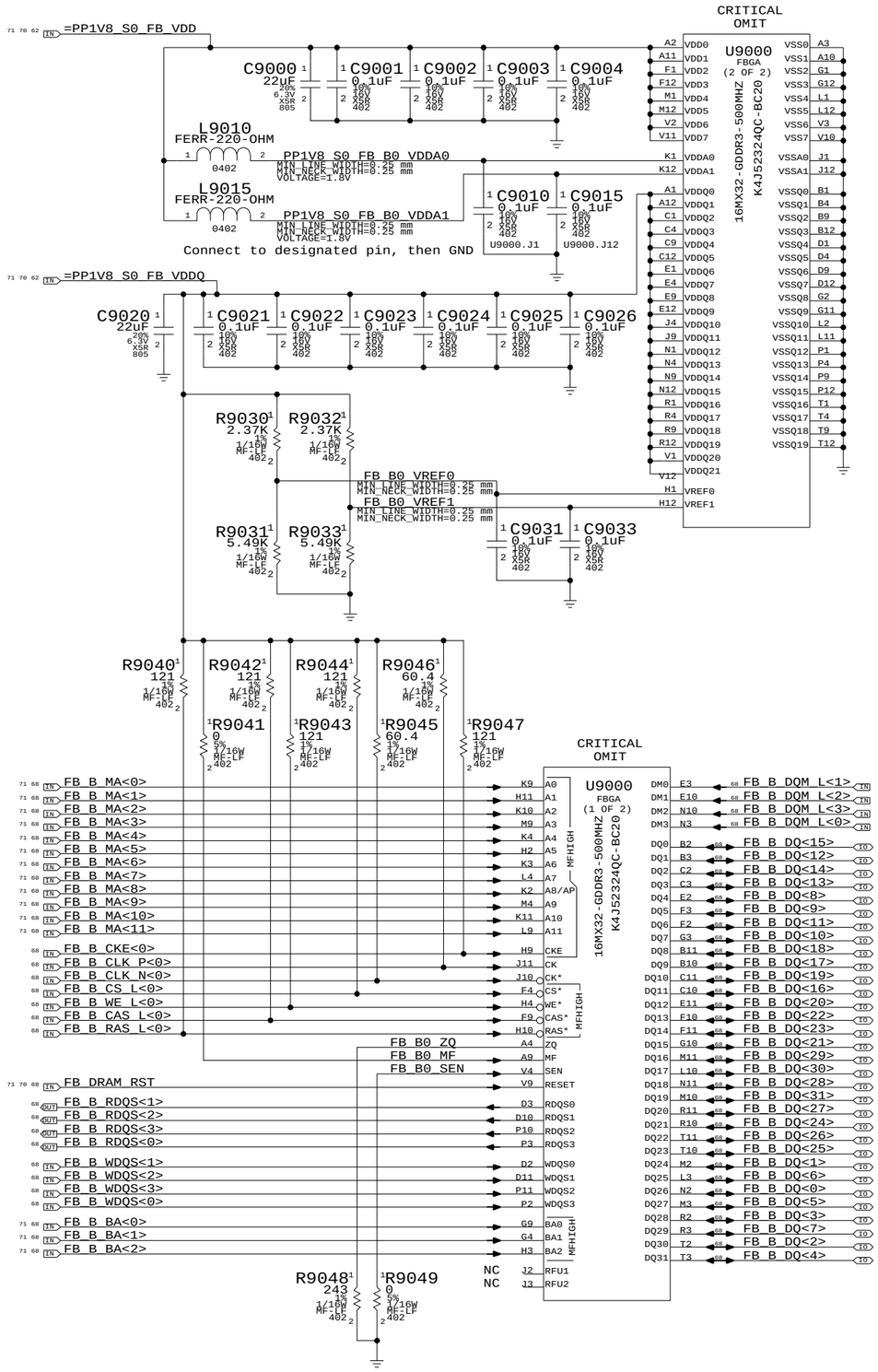
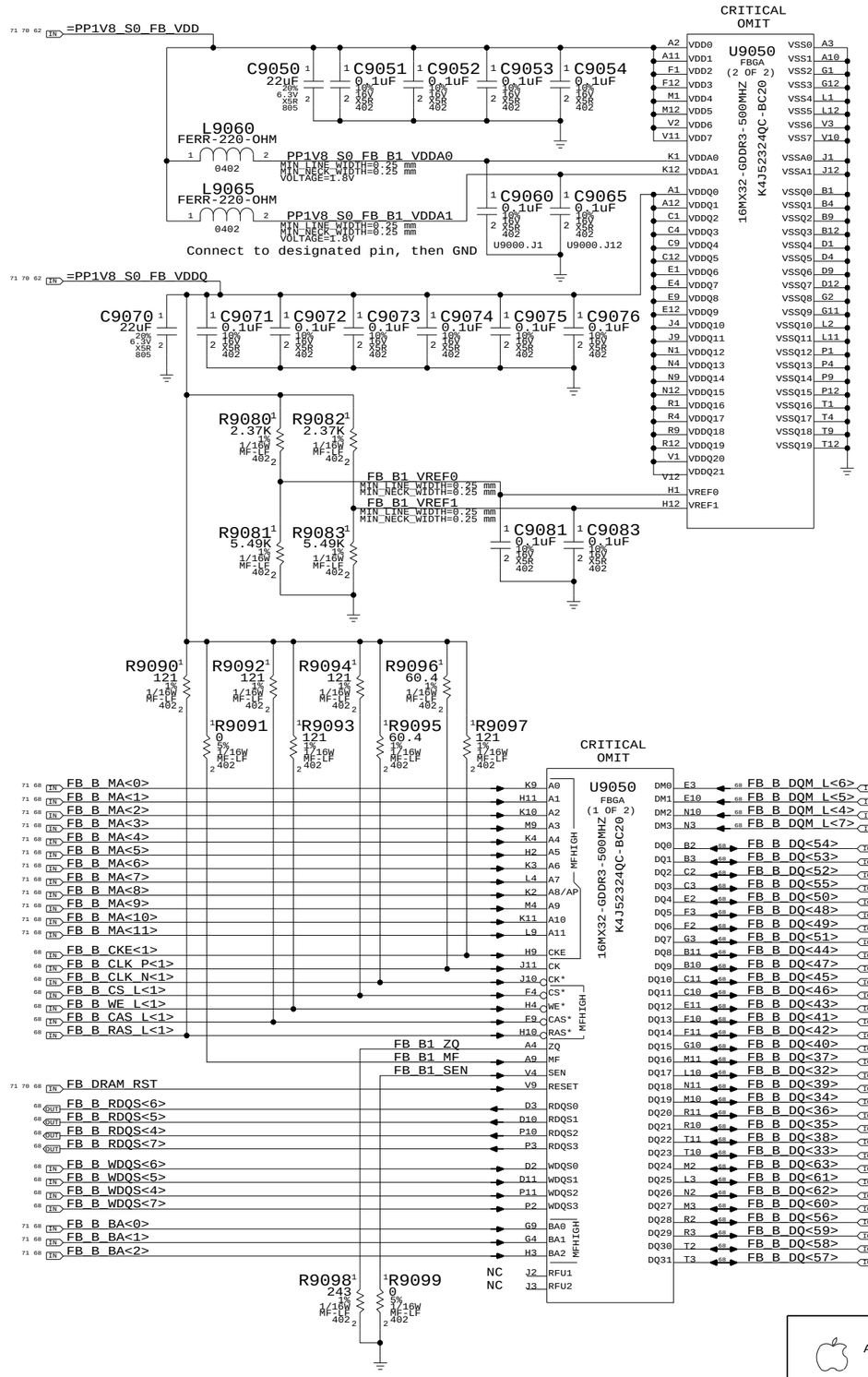
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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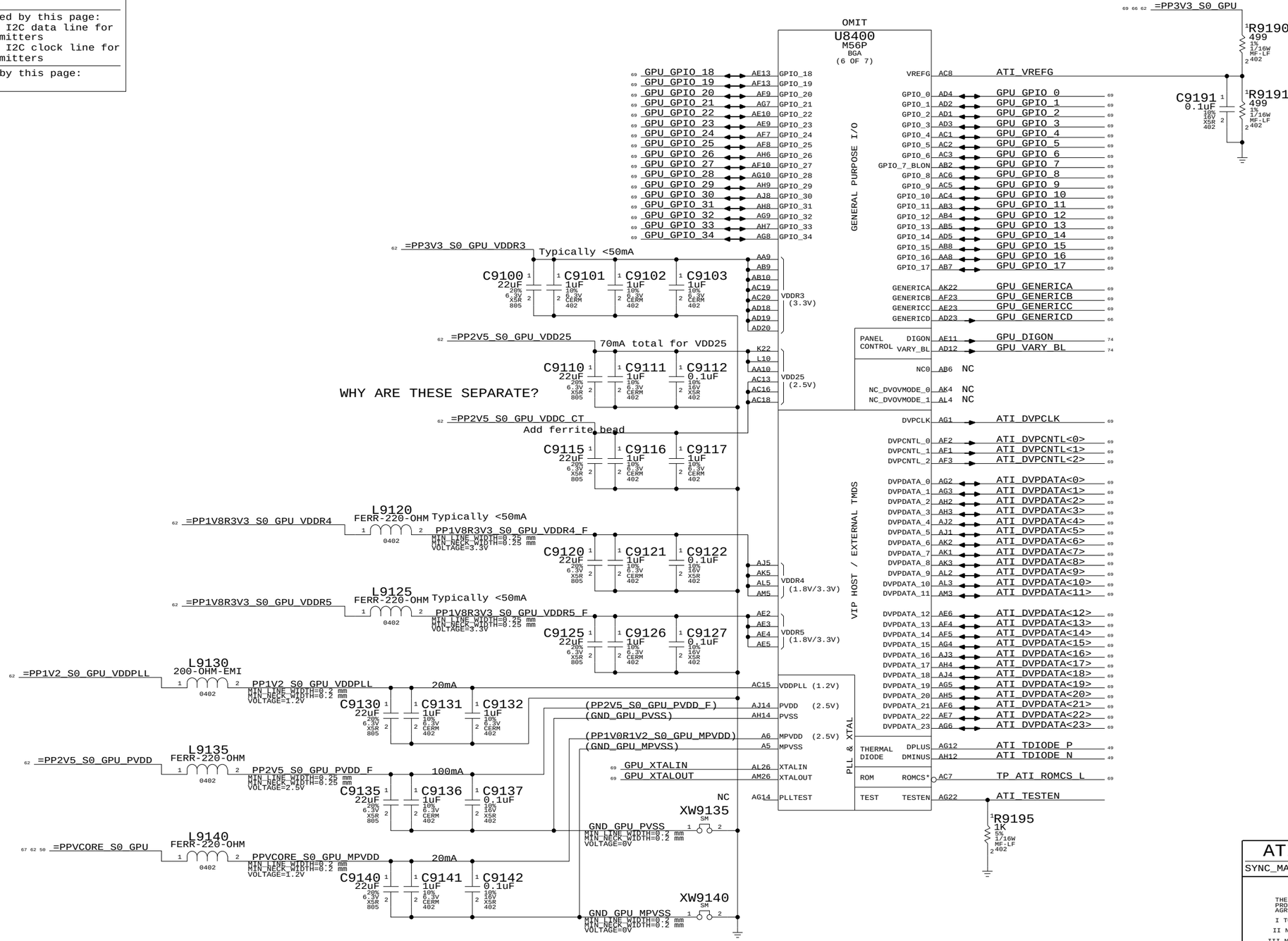
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

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Page Notes

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- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

62 =PP2V5_S0_GPU

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 XW9300 SM — PP2V5_S0_GPU_TPVDD — 20mA peak
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=2.5V
C9300 22uF 20% 6.3V X5R 805 | C9301 1uF 10% 6.3V CERM 402 | C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 XW9305 SM — PP2V5_S0_GPU_TXVDDR — 150mA peak
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.5V
C9305 22uF 20% 6.3V X5R 805 | C9306 1uF 10% 6.3V CERM 402 | C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 XW9310 SM — PP2V5_S0_GPU_AVDD — 65mA peak
MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.5V
C9310 22uF 20% 6.3V X5R 805 | C9311 1uF 10% 6.3V CERM 402 | C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — 20mA peak
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=2.5V
C9315 22uF 20% 6.3V X5R 805 | C9316 1uF 10% 6.3V CERM 402 | C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 XW9320 SM — PP2V5_S0_GPU_A2VDD — 130mA peak
MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.5V
C9320 22uF 20% 6.3V X5R 805 | C9321 1uF 10% 6.3V CERM 402 | C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 XW9324 SM — PP2V5_S0_GPU_VDD2DI — 20mA peak
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=2.5V
C9325 22uF 20% 6.3V X5R 805 | C9326 1uF 10% 6.3V CERM 402 | C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 XW9330 SM — PP2V5_S0_GPU_LPVDD — 20mA peak
MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=2.5V
C9330 22uF 20% 6.3V X5R 805 | C9331 1uF 10% 6.3V CERM 402 | C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 XW9345 SM — PP2V5_S0_GPU_LVDDR — 200mA peak
MIN_LINE_WIDTH=0.35 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=2.5V
C9340 22uF 20% 6.3V X5R 805 | C9345 22uF 20% 6.3V X5R 805 | C9341 1uF 10% 6.3V CERM 402 | C9342 0.1uF 10% 16V X5R 402 | C9346 0.1uF 10% 16V X5R 402 | C9347 0.1uF 10% 16V X5R 402

GND_GPU_TPVSS — MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V
GND_GPU_TXVSSR — MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V
GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V
GND_GPU_AVSSQ — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V
GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V
GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V
GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=0V
GND_GPU_LVSSR — MIN_LINE_WIDTH=0.35 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V

OMIT
U8400 M56P BGA (5 OF 7)

AM8	TPVDD (2.5V)		
AL8	TPVSS		
AJ6	TXVDDR (2.5V)		INTEGRATED TMDS
AK6			
AL6			
AM6			
AJ7	TXVSSR		
AK7			
AK8			
AL7			
AM7			
AL25	AVDD (2.5V)		
AM25			
AJ24	AVSS		
AK25			
AK23	AVSSQ		
AM23	VDD1DI (2.5V)		
AL23	VSS1DI		
AL22	RSET		DAC (CRT)
AL16	A2VDD (2.5V)		
AM16			
AL17	A2VSS		
AM17			
AL14	NC_A2VDDQ		DAC2 (TV/CRT2)
AK13	A2VSSQ		
AJ16	VDD2DI (2.5V)		
AJ17	VSS2DI		
AK14	R2SET		
AE19	LPVDD (2.5V)		
AE18	LPVSS		
AC21	LVDDR (2.5V)		LVDS
AC22			
AD21			
AD22			
AE20			
AE21			
AE22			
AF19			
AF20			
AF17	LVSSR		
AF18			
AF21			
AF22			
AG17			
AG19			
AH17			
AH19			
AJ19			
AK17			
AF11	HPD1		MONITOR IDENTIFICATION

ATI_RSET (73) — ATI_R2SET (73)
R9350 499 1% 1/16W MF-LF 402 — R9351 715 1% 1/16W MF-LF 402

GPU_HPD (75, IN)

TXCP	AM9	81 75 74	TMDS_CLK_P
TXCM	AL9	81 75 74	TMDS_CLK_N
TX0P	AL10	81 75 74	TMDS_DATA_P<0>
TX0M	AK10	81 75 74	TMDS_DATA_N<0>
TX1P	AM11	81 75 74	TMDS_DATA_P<1>
TX1M	AL11	81 75 74	TMDS_DATA_N<1>
TX2P	AM12	81 75 74	TMDS_DATA_P<2>
TX2M	AL12	81 75 74	TMDS_DATA_N<2>
TX3P	AJ9	81 75 74	TMDS_DATA_P<3>
TX3M	AK9	81 75 74	TMDS_DATA_N<3>
TX4P	AJ11	81 75 74	TMDS_DATA_P<4>
TX4M	AK11	81 75 74	TMDS_DATA_N<4>
TX5P	AJ12	81 75 74	TMDS_DATA_P<5>
TX5M	AK12	81 75 74	TMDS_DATA_N<5>
R	AK24	69	GPU_VGA_R
G	AM24	69	GPU_VGA_G
B	AL24	69	GPU_VGA_B
HSYNC	AJ23	69	GPU_VGA_HSYNC
VSYNC	AJ22	69	GPU_VGA_VSYNC
R2	AK15	75 74	GPU_R2
G2	AM15	75 74	GPU_G2
B2	AL15	75 74	GPU_B2
H2SYNC	AE15	75	GPU_H2SYNC
V2SYNC	AG15	75	GPU_V2SYNC
Y	AJ15	69	GPU_TV_Y
C	AJ13	69	GPU_TV_C
COMP	AH15	69	GPU_TV_COMP
TXCLK_UP	AJ21	74	LVDS_U_CLK_P
TXCLK_UN	AK21	74	LVDS_U_CLK_N
TXOUT_U0P	AG18	74	LVDS_U_DATA_P<0>
TXOUT_U0N	AH18	74	LVDS_U_DATA_N<0>
TXOUT_U1P	AK20	74	LVDS_U_DATA_P<1>
TXOUT_U1N	AJ20	74	LVDS_U_DATA_N<1>
TXOUT_U2P	AG20	74	LVDS_U_DATA_P<2>
TXOUT_U2N	AH20	74	LVDS_U_DATA_N<2>
TXOUT_U3P	AH21	69	LVDS_U_DATA_P<3>
TXOUT_U3N	AG21	69	LVDS_U_DATA_N<3>
TXCLK_LP	AM18	74	LVDS_L_CLK_P
TXCLK_LN	AL18	74	LVDS_L_CLK_N
TXOUT_L0P	AL19	74	LVDS_L_DATA_P<0>
TXOUT_L0N	AK19	74	LVDS_L_DATA_N<0>
TXOUT_L1P	AM20	74	LVDS_L_DATA_P<1>
TXOUT_L1N	AL20	74	LVDS_L_DATA_N<1>
TXOUT_L2P	AM21	74	LVDS_L_DATA_P<2>
TXOUT_L2N	AL21	74	LVDS_L_DATA_N<2>
TXOUT_L3P	AJ18	69	LVDS_L_DATA_P<3>
TXOUT_L3N	AK18	69	LVDS_L_DATA_N<3>
DDC1CLK	AH23	75	GPU_DDC_A_CLK
DDC1DATA	AH22	75	GPU_DDC_A_DATA
DDC2CLK	AG13	69	GPU_DDC_B_CLK
DDC2DATA	AH13	69	GPU_DDC_B_DATA
DDC3CLK	AF12	74	GPU_DDC_C_CLK
DDC3DATA	AE12	74	GPU_DDC_C_DATA

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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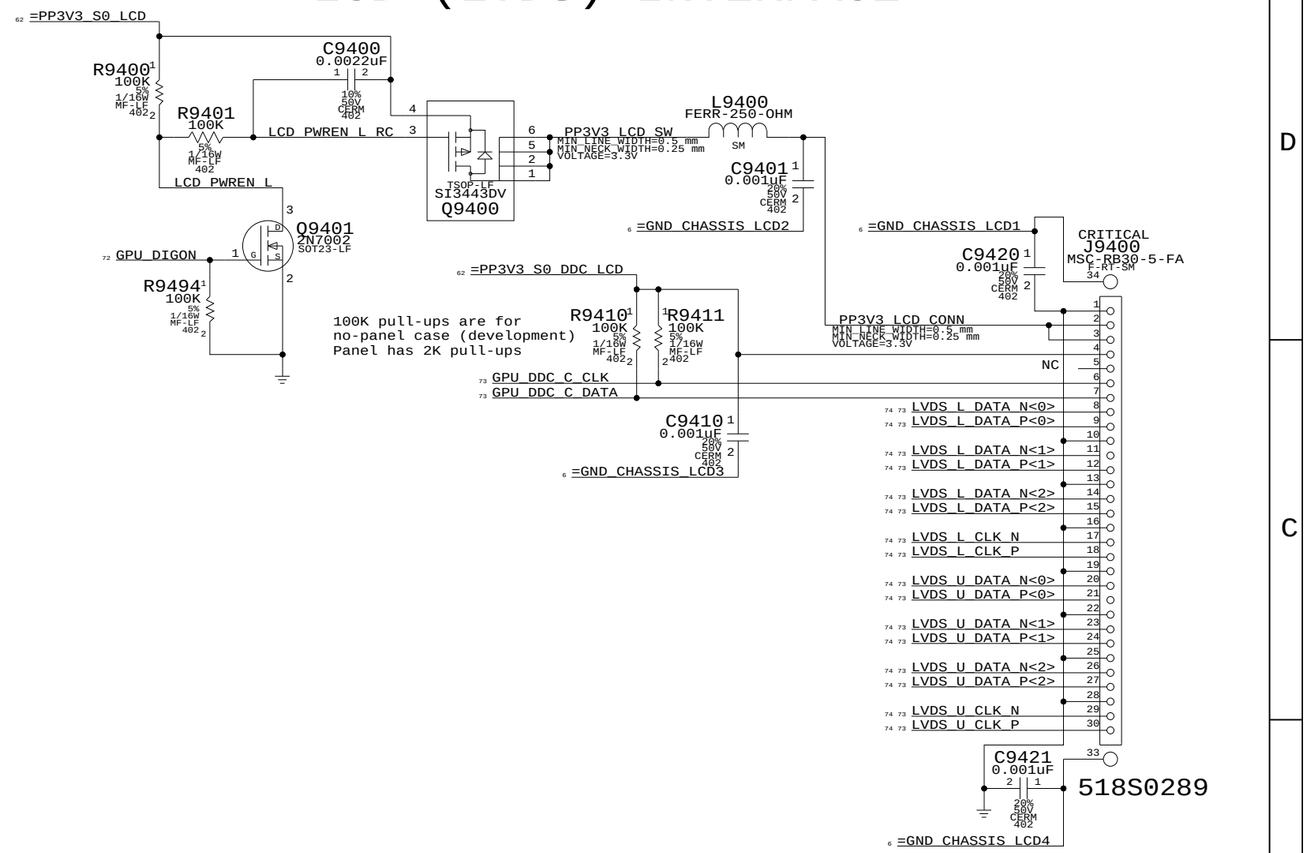
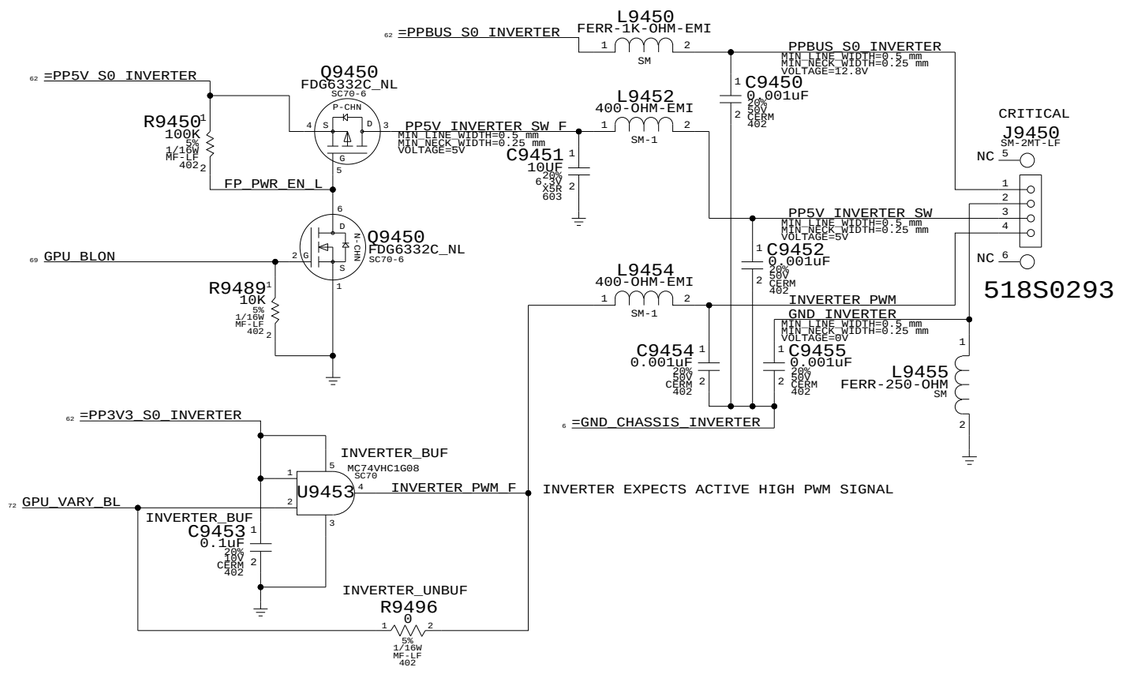
LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
	VGA	VGA	GPU_R2
	VGA	VGA	GPU_G2
	VGA	VGA	GPU_B2
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_N<2..0>
	TMDS	TMDS	TMDS_CLK_P
	TMDS	TMDS	TMDS_CLK_N
	TMDS	TMDS	TMDS_DATA_P<5..3>
	TMDS	TMDS	TMDS_DATA_N<5..3>
	TMDS	TMDS	TMDS_DATA_P<2..0>
	TMDS	TMDS	TMDS_DATA_N<2..0>



INVERTER INTERFACE



Internal Display Connectors

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TMDS Filtering

Place series R's close to GPU, other parts near connector.

TMDS_DATA_N<0>	R9760 0	TMDS_DATA_R_N<0>	TMDS_DATA_F_N<0>
TMDS_DATA_P<0>	R9761 0	TMDS_DATA_R_P<0>	TMDS_DATA_F_P<0>
	R9762 49.9 1%	R9763 49.9 1%	
	C9762 0.001uF	TMDS_D0_CMF	
TMDS_DATA_N<1>	R9764 0	TMDS_DATA_R_N<1>	TMDS_DATA_F_N<1>
TMDS_DATA_P<1>	R9765 0	TMDS_DATA_R_P<1>	TMDS_DATA_F_P<1>
	R9766 49.9 1%	R9767 49.9 1%	
	C9766 0.001uF	TMDS_D1_CMF	
TMDS_DATA_N<2>	R9768 0	TMDS_DATA_R_N<2>	TMDS_DATA_F_N<2>
TMDS_DATA_P<2>	R9769 0	TMDS_DATA_R_P<2>	TMDS_DATA_F_P<2>
	R9770 49.9 1%	R9771 49.9 1%	
	C9770 0.001uF	TMDS_D2_CMF	
TMDS_CLK_N	R9772 0	TMDS_CLK_R_N	TMDS_CLK_F_P
TMDS_CLK_P	R9773 0	TMDS_CLK_R_P	TMDS_CLK_F_N
	R9774 49.9 1%	R9775 49.9 1%	
	C9774 0.001uF	TMDS_CLK_CMF	
TMDS_DATA_N<3>	R9776 0	TMDS_DATA_R_N<3>	TMDS_DATA_F_N<3>
TMDS_DATA_P<3>	R9777 0	TMDS_DATA_R_P<3>	TMDS_DATA_F_P<3>
	R9778 49.9 1%	R9779 49.9 1%	
	C9778 0.001uF	TMDS_D3_CMF	
TMDS_DATA_N<4>	R9780 0	TMDS_DATA_R_N<4>	TMDS_DATA_F_N<4>
TMDS_DATA_P<4>	R9781 0	TMDS_DATA_R_P<4>	TMDS_DATA_F_P<4>
	R9782 49.9 1%	R9783 49.9 1%	
	C9782 0.001uF	TMDS_D4_CMF	
TMDS_DATA_N<5>	R9784 0	TMDS_DATA_R_N<5>	TMDS_DATA_F_N<5>
TMDS_DATA_P<5>	R9785 0	TMDS_DATA_R_P<5>	TMDS_DATA_F_P<5>
	R9786 49.9 1%	R9787 49.9 1%	
	C9786 0.001uF	TMDS_D5_CMF	

All series R: 0, 5%, 1/10W, MF-LF, 402. All caps: 10%, 50V, CERM, 402.

CRITICAL	L9700 90-OHM-300mA, 2012H, SYM_VER-1
CRITICAL	L9701 90-OHM-300mA, 2012H, SYM_VER-1
CRITICAL	L9702 90-OHM-300mA, 2012H, SYM_VER-1
CRITICAL	L9706 370-OHM, SM, SYM_VER-1
CRITICAL	L9703 90-OHM-300mA, 2012H, SYM_VER-1
CRITICAL	L9704 90-OHM-300mA, 2012H, SYM_VER-1
CRITICAL	L9705 90-OHM-300mA, 2012H, SYM_VER-1

VGA SYNC BUFFERS

=PP3V3_S0_VGASYNC → U9750 (MC74VHC1G08, SC70) ← GPU_V2SYNC; C9750 0.1uF, 20%, 10V, CERM, 402

U9750 VGA_VSYNC_R → R9750 33, 5%, 1/10W, MF-LF, 402 → VGA_VSYNC

=PP3V3_S0_VGASYNC → U9751 (MC74VHC1G08, SC70) ← GPU_H2SYNC; C9751 0.1uF, 20%, 10V, CERM, 402

U9751 VGA_HSYNC_R → R9751 33, 5%, 1/10W, MF-LF, 402 → VGA_HSYNC

PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

=PP5V_S0_DVI_DDC → CRITICAL F9710 0.5AMP-13.2V, SM-LF → PP5V_S0_DDC_F

L9710 400-OHM-EMI, SM-1: PP5V_S0_DDC_F → PP5V_S0_DDC

VOLTAGE=5V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm

DVI INTERFACE

CRITICAL J9700 QH11121-RIG02-4F, F-RT-TH-DVI

=GND_CHASSIS_DVI1	33	31	
TMDS_DATA_F_N<0>	17	1	TMDS_DATA_F_N<2>
	9		TMDS_DATA_F_N<1>
TMDS_DATA_F_P<0>	18	2	TMDS_DATA_F_P<2>
	10		TMDS_DATA_F_P<1>
	19	3	
		11	
TMDS_DATA_F_N<5>	20	4	TMDS_DATA_F_N<4>
	12		TMDS_DATA_F_N<3>
TMDS_DATA_F_P<5>	21	5	TMDS_DATA_F_P<4>
	13		TMDS_DATA_F_P<3>
	22	6	DVI_DDC_CLK_R
	14		(PP5V_S0_DDC)
TMDS_CLK_F_P	23	7	DVI_DDC_DATA_R
	15		
TMDS_CLK_F_N	24	8	VGA_VSYNC
	16		DVI_HPD_R
VGA_B	C3	C1	VGA_R
	C5B	C5A	
VGA_HSYNC	C4	C2	VGA_G
	34	32	
=GND_CHASSIS_DVI2			

514-0278

PLACE NEAR C5A & C5B

R9730 0, 5%, 1/10W, MF-LF, 402 → =GND_CHASSIS_DVI3

R9731 0, 5%, 1/10W, MF-LF, 402 → =GND_CHASSIS_DVI4

PLACE NEAR 3, 11 & 19

Isolation required for DVI power switch

D9710 SOD-123: B0530WXF

PP5V_S0_DDC_PULLUPS (VOLTAGE=5V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm)

R9710 4.7K, R9712 4.7K, 5%, 1/10W, MF-LF, 402

C9710 0.01uF, 20%, 50V, CERM, 603

C9711 100pF, C9713 100pF, C9714 100pF, 5%, 50V, CERM, 402

3V LEVEL SHIFTERS

=PP3V3_S0_DDC_DVI

DVI_DDC_CLK	R9711 100, 5%, 1/10W, MF-LF, 402	Q9711 2N7002DW-X-F, SOT-363	GPU_DDC_A_CLK
DVI_DDC_DATA	R9713 100, 5%, 1/10W, MF-LF, 402	Q9711 2N7002DW-X-F, SOT-363	GPU_DDC_A_DATA
DVI_HPD	R9714 100, 5%, 1/10W, MF-LF, 402	Q9714 2N7002DW-X-F, SOT-363	GPU_HPD

R9720 10K, R9721 10K, R9722 100K, 5%, 1/16W, MF-LF, 402

R9715 20K, 5%, 1/10W, MF-LF, 402

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

GPU_B2 (DAC2 Comp)	R9740 75, 1%, 1/10W, MF-LF, 402	CRITICAL FL9740 LCFILTER SM-220MHZ-LF	VGA_B
GPU_G2 (DAC2 Y)	R9741 75, 1%, 1/10W, MF-LF, 402	CRITICAL FL9741 LCFILTER SM-220MHZ-LF	VGA_G
GPU_R2 (DAC2 C)	R9742 75, 1%, 1/10W, MF-LF, 402	CRITICAL FL9742 LCFILTER SM-220MHZ-LF	VGA_R

C9740 3.3pF, C9741 3.3pF, C9742 3.3pF, 0.25%, 50V, CERM, 402

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	
	TMDS	TMDS	TMDS_CLK_R_P
	TMDS	TMDS	TMDS_CLK_R_N
	TMDS	TMDS	TMDS_DATA_R_P<5..0>
	TMDS	TMDS	TMDS_DATA_R_N<5..0>
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..0>

External Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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Secure Signal List

Nets must be buried with no exposed vias between parts listed in SECURE_NET property. No test points allowed between the secure devices, test points are allowed past the secure devices except on nets marked as NO_TEST=TRUE, no test points are allowed on those nets.

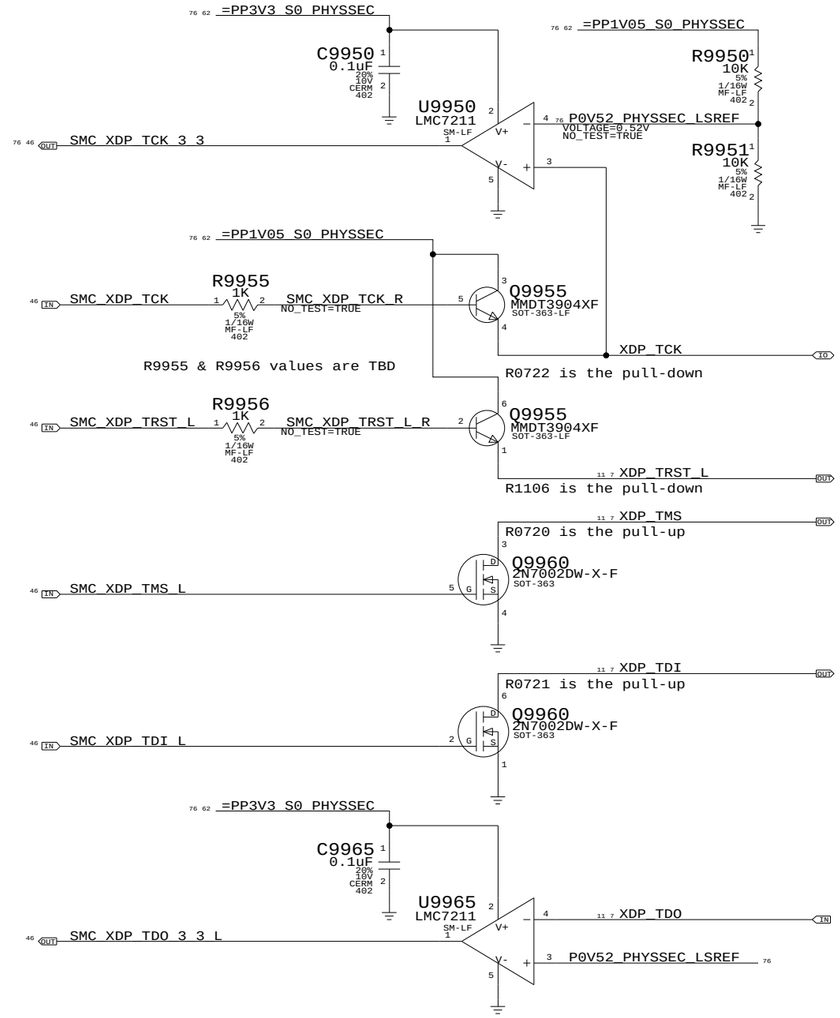
SECURE_NET=U2100:U5800		SPI_CE_L	22 46 51
SECURE_NET=U2100:U5800		SPI_SO	22 46 51
SECURE_NET=U2100:U5800		SPI_SI	22 46 51
SECURE_NET=U2100:U5800	NO_TEST=TRUE	SPI_ARB	22 46
SECURE_NET=U5800:U7530		BOOT_LPC_SPI_L	5 22 46 48
SECURE_NET=U5800:U7530		IMVP_VR_ON	46 56
SECURE_NET=U0700:U9950:Q9955		XDP_TCK	7 11 76
SECURE_NET=U9950:U5800		SMC_XDP_TCK_3_3	46 76
SECURE_NET=U5800:R9955		SMC_XDP_TCK_L	
SECURE_NET=R9955:Q9955		SMC_XDP_TCK_L_R	

NEED TO TURN PCI_GNT3_L INTO A NC NET!

SMC <-> CPU JTAG Level-Shifting

ALL OF THESE PARTS WILL BE COVERED IN EPOXY

Place these parts on one side and as close together as possible, and keep enough room from other parts to leave room for epoxy covering. Nets that are local to this circuit do not need test points as they will not be accessible.



Physical Security

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NONE	76	81

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Date - Radar # - Description

DMS Release #03000 (RFA #394758)

2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.

Changes from Proto Branch (DMS Release #04000):

2005/08/27 - 4230219 - Changed Y3301 to non-obsoleted part.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.
2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.
2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.
2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.
2005/08/28 - 4217535 - Added Left ALS FFC connector.
2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.
2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.
2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).
2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.
2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.
2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.
2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.

DMS Checkin #04001

2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.
2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.
2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.
2005/08/29 - 4227336 - Changed Y5920 to 197S0169.
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).
2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.
2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).
2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.

DMS Checkin #04002

2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.

DMS Checkin #04003

2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.
2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500.
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.

DMS Checkin #04004

2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.

DMS Checkin #04005

2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.

DMS Checkin #04006

2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.
2005/09/03 - 4232534 - Added notes for power supplies and connectors.

DMS Checkin #04007

2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.
2005/09/06 - 4246683 - Removed NO_STUFF option from R8805 per ATI request.
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.

DMS Release #05000-07000 (Proto 2 releases)

2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.
2005/09/08 - 4248911 - Sync with M38 & M42
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR	*	=3:1_SPACING
FSB_ADDR2ADDR	*	=2:1_SPACING
FSB_ADSTB	*	=3:1_SPACING
FSB_ADDR2ADSTB	*	=3:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_DATA	*	=3:1_SPACING
FSB_DATA2DATA	*	=2:1_SPACING
FSB_DSTB	*	=3:1_SPACING
FSB_DATA2DSTB	*	=3:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_COMMON	*	=2:1_SPACING

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CPU_2TO1	*	=2:1_SPACING
CPU_COMP	*	25 MIL
CPU_GTLREF	*	25 MIL
CPU_ITP	*	=2:1_SPACING
CPU_VCCSENSE	*	25 MIL

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_CLK2MEM	*	=4:1_SPACING
MEM_CTRL2CTRL	*	=2:1_SPACING
MEM_CTRL2MEM	*	=3:1_SPACING
MEM_CMD2CMD	*	=1.5:1_SPACING
MEM_CMD2MEM	*	=3:1_SPACING
MEM_DATA2DATA	*	=1.5:1_SPACING
MEM_DATA2MEM	*	=3:1_SPACING
MEM_DQS2MEM	*	=3:1_SPACING
MEM_2OTHER	*	25 MIL

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCIE	*	20 MIL
DMI	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
IDE	*	=1.8:1_SPACING
SATA	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
AUDIO	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
USB2	*	=4:1_SPACING
USB2_2CLK	*	25 MIL

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
SMB	*	=3:1_SPACING
SPI	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	*	25 MIL
CLK_PCIE	*	20 MIL
CLK_MED	*	20 MIL
CLK_SLOW	*	10 MIL

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FB_ADCTRL	*	=2.5:1_SPACING
FB_CLK	*	=2.5:1_SPACING
FB_DATA	*	=2.5:1_SPACING

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS	*	=3:1_SPACING
TMDS	*	=3:1_SPACING
VGA	*	15 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS_PAIR2PAIR	*	25 MIL
TMDS_PAIR2PAIR	*	25 MIL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
ENET	*	=3:1_SPACING
FW	*	=3:1_SPACING

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCI	*	=2:1_SPACING

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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M1 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.076 MM	0.076 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
DEFAULT	*	0.1 MM
STANDARD	*	=DEFAULT
BGA_P1MM	*	=DEFAULT
BGA_P2MM	*	=DEFAULT
BGA_P3MM	*	=DEFAULT

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	*	0.15 MM
1.8:1_SPACING	*	0.18 MM
2:1_SPACING	*	0.2 MM
2.5:1_SPACING	*	0.25 MM
3:1_SPACING	*	0.3 MM
4:1_SPACING	*	0.4 MM

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	ISL2,ISL11	0.1 MM
1.8:1_SPACING	ISL2,ISL11	0.1 MM
2:1_SPACING	ISL2,ISL11	0.1 MM
2.5:1_SPACING	ISL2,ISL11	0.1 MM
3:1_SPACING	ISL2,ISL11	0.1 MM
4:1_SPACING	ISL2,ISL11	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	ISL2,ISL11	0.1 MM
CLK_PCIE	ISL2,ISL11	0.1 MM
CLK_MED	ISL2,ISL11	0.1 MM
CLK_SLOW	ISL2,ISL11	0.1 MM
CPU_COMP	ISL2,ISL11	0.1 MM
CPU_GTLREF	ISL2,ISL11	0.1 MM
CPU_VCCSENSE	ISL2,ISL11	0.1 MM
DMI	ISL2,ISL11	0.1 MM
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM
MEM_2OTHER	ISL2,ISL11	0.1 MM
PCIE	ISL2,ISL11	0.1 MM
SATA	ISL2,ISL11	0.1 MM
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM
VGA	ISL2,ISL11	0.1 MM

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M1 Spacing & Physical Constraints

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12 47
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 56
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	56
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 81
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 81
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 56
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	56

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 44
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 44

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

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